Tektronix Logic Analyzers

TLA7000 Series Data Sheet

Features & Benefits

- 68/102/136 Channel Logic Analyzers with up to 512 Mb Record Length
- MagniVu™ Acquisition Technology provides up to 20 ps (50 GHz) Timing Resolution to Find and Measure Elusive Timing Problems Quickly
- Up to 156 ps (6.4 GHz)/512 Mb Record Length Timing Analysis
- Up to 1.4 GHz Clock with up to 3.0 Gb/s Data with a Data Valid Window of 180 ps for State Acquisition Analysis of High-performance Synchronous Buses
- Glitch and Setup/Hold Triggering and Display Finds and Displays Elusive Hardware Problems
- Transitional Storage Extends the Signal Analysis Capture Time for Signals that Transition Infrequently
- Simultaneous State, High-speed Timing, and Analog Analysis through the Same Probe Pinpoints Elusive Faults
- Compression Probing System With 0.5 pF Capacitive Loading Eliminates Need for Onboard Connectors, Minimizes Intrusion on Circuits, and is Ideal for Differential Signal Applications
- Trace Problems from Symptom back to Root Cause in Real-time Across Multiple Modules by Viewing Time-correlated Data in a Wide Variety of Display Formats
- 8/16 Channel Serial Analyzer Modules with 32M 8b/10b Symbol Memory Depth per Channel
- 2.5 Gb/s and 5 Gb/s Acquisition Speed for PCI Express 1.0 and PCI Express 2.0
- Mid-bus Probes Connectorless Probing System supports acquisition of PCI Express 1.0 and PCI Express 2.0 up to 5.0 Gb/s
- Solder-down Probes supports PCI Express 1.0 and PCI Express 2.0 up to 5.0 Gb/s
- Modular Mainframes Provide Flexibility and Expandability
- Supports up to 6,528 Logic Analyzer Channels, 48 Independent Buses
- Broad Processor and Bus Support

Applications

- FPGA Debug and Verification
- MIPI Protocol Analysis
- DDR2 and DDR3 Debug and Verification
- Signal Integrity
- PCI Express Validation for:
  - Silicon Validation
  - Computer System Validation
  - Embedded System Debug and Validation
- Processor/Bus Debug and Verification
- Embedded Software Integration, Debug, and Verification

Breakthrough Solutions for Real-time Digital Systems Analysis

Tektronix provides breakthrough digital systems analysis tools that enable digital hardware and software designers to capture and analyze the source of elusive problems that threaten product development schedules. The TLA7000 Series provides the speed you need to capture the source of those elusive problems, plus the visibility you want with large displays and fast system data throughput, while protecting your investment with compatibility with all TLA modules.

Tektronix®

TLA7012 and TLA7016 Mainframes

The TLA7012 Portable and TLA7016 Benchtop mainframes are modular mainframes that accept TLA logic analyzer and pattern generator modules. The TLA7012 and TLA7016 can be configured as either master or expansion mainframes to provide solutions for large numbers of buses and high channel-count requirements.

The TLA7012 Portable Mainframe and TLA7016 Benchtop Mainframe along with the TLAPC1 Benchtop Controller are built on a Microsoft Windows XP Professional PC platform that offers a familiar work environment for the TLA application software. They provide multiple display capability for extended desktop viewing, in addition to an internal DVD-RW, hard drive, and multiple USB 2.0 ports for expansion. A replaceable hard drive is standard on both mainframes, ideal for security or enabling individual team members to store personal setups and data. Trigger in/out connections provide an interface to other external instrumentation, such as DPO oscilloscopes, for correlating measurement results.

TLA7ACx and TLA7Bxx Modules

Today's digital design engineers face daily pressures to speed new products to the marketplace. The TLA7ACx and TLA7Bxx Series logic analyzer modules answer the need with breakthrough solutions for the entire design team, providing the ability to quickly monitor, capture, and analyze real-time digital system operation in order to debug, verify, optimize, and validate digital systems. Hardware developers, hardware/software integrators, and embedded software developers will appreciate the range of capabilities of the TLA7ACx and TLA7Bxx Series logic analyzer modules. Its broad feature set includes capturing and correlating elusive hardware and software faults; providing simultaneous state, high-speed timing, and analog analysis through the same probe; using deep state acquisition to find the cause of complex problems; real-time, nonintrusive software execution tracing that correlates to source code and to hardware events; and nonintrusive connectorless probing.

The TLA7Bxx Series logic analyzer modules offer Tektronix' breakthrough MagniVu™ technology for providing high-speed sampling (up to 50 GHz) that dramatically changes the way logic analyzers work and enables them to provide startling new measurement capabilities. The TLA7Bxx modules offer high-speed state synchronous capture, high-speed timing capture, and analog capture through the same set of probes. They capitalize on MagniVu technology to offer up to 20 ps timing on all channels, glitch and setup/hold triggering, and display and time stamp that is always on at up to 20 ps resolution.

To compliment the high-performance logic analyzer modules, the TLA7ACx Series logic analyzer modules offers all the same debug and verification functionality, but with performance levels more suited to the embedded designer. The TLA7ACx modules offer high-speed state synchronous capture, high-speed timing capture, and analog capture through the same set of probes. MagniVu technology offering up to 125 ps timing on all channels, glitch and setup/hold triggering, and display and time stamp that is always on at 125 ps resolution is available as standard on all models.

Module	Timing Resolution	State Speed	Memory
TLA7ACx	125 ps (8 GHz)	Up to 800 MHz	Up to 128 Mb
TLA7Bxx	20 ps (50 GHz)	Up to 1.4 GHz	Up to 128 Mb

P68xx and P69xx Probes

No test and measurement solution is complete without probing. With the industry's lowest capacitance, the P6800 and P6900 Series logic analyzer probes protect the integrity of your signal – critical for connecting to fast buses like DDR2 and DDR3 where low intrusion is key to the proper operation of your design. Select from single-ended and differential probes and a variety of attachment mechanisms, including the "connectorless" compression connection that eliminates the need for onboard connectors.

For applications where circuit board space is at a premium, the high-density P6900 Series with D-Max® Probing Technology offers the industry's smallest available footprint. For debugging the signal integrity glitches common on fast buses, the P6900 Series works with the TLA7Bxx and TLA7ACx modules and their iLink™ Tool Set capability to provide iCapture™ simultaneous digital-analog acquisition. This allows you to clearly see the time-correlated digital and analog behavior of your design, without the extra capacitance and setup time of double-probing.

For differential signaling applications where signal integrity is critical, the high-fidelity P6980 and P6982 are perfect for those applications where noise performance is critical. In addition, the P6980 and P6982 can support the small voltage swings that differential signaling often requires. The P6962DBL, when used with a TLA7000 logic analyzer with the TLA7Bxx module, supports digital validation and debug of DDR3 memory with data rates up to 1600 mega-transfers per second. For board designs that do not include high-density probe footprints, the P6960 with its companion flying leadset provides the flexibility required to meet many different debug needs.

TLA7Sxx PCI Express Gen 2 Modules

PCI Express 2.0 introduces new challenges for validation engineers. Time-to-market pressures require a solution that can quickly pinpoint problems. The TLA7Sxx Series serial analyzer modules provide an innovative approach to PCI Express validation that spans all layers of the protocol from the physical layer to the transaction layer.

For the first time, parallel and serial acquisition modules can be utilized in both the TLA7012 Portable Mainframe and the TLA7016 Benchtop Mainframe offering the highest degree of flexibility. Additionally, the TLA7Sxx Series serial analyzer modules have unsurpassed ability to capture and trigger on PHY layer events, whether problems exist during link training or while the link is going into or out of power management states. Complete support for L0 and L1 power management is critical as power-saving techniques become more prevalent in system designs. The TLA7Sxx Series serial analyzer acquisition capability is complemented by analysis tools which provide protocol decode and error reporting capabilities.

Hardware developers, hardware/software integrators, and embedded system designers will appreciate the tight integration with the Tektronix Logic Analyzer. Correlation with other system buses or general-purpose debug signals uses the TLA common-system time stamp. Elusive problems that may have been propagated from other system buses can be efficiently debugged in a single environment. Coupled with the P67xx Series mid-bus probes, engineers have flexible options for platform accessibility.

P67xx Series Probes for PCI Express Gen 2

The P67xx Series probes provide validation engineers with two mid-bus probing options and one solder-down option. The P67xx mid-bus probes are the best choice for minimal system impact. The P67xx use a new “connectorless” retention mechanism that is designed to maximize mechanical reliability. Conserving circuit board space is critical, the P6708 8-channel half-width probe is an ideal choice for designs that use x1 and x4 links. The P6716 16-channel full-width probe is also available. The P6701SD enables customers to validate their PCI Express designs on platforms where no mid-bus or slot connector exists.

TLA7012 and TLA7016 Characteristics

General

Characteristic	Description
Instrument Slots	TLA7012: Holds 2 TLA modules. TLA7016: Holds 6 TLA modules.
Expansion Capability	The TLA7000 Series mainframes can be used as either master or expansion mainframes (TL708EX 8-port Instrument Hub and Expander is required for 3-8 mainframes connected together using TekLink™ cable). TLA7012: Up to eight TLA7012 mainframes can be used providing support for up to 16 TLA modules (2,176 channels). TLA7016: Up to eight TLA7016 mainframes can be used providing support for up to 48 TLA modules (6,528 channels).

TLA7012 PC Characteristics

Characteristic	Description
Operating System	Microsoft® Windows® XP Professional and Multilingual User Interface Pack.
Processor	2 GHz Intel® Pentium® M-760.
Chipset	Intel® 915GM.
Memory	1 GB DDR PC 533 MHz (SODIMM), expandable to 2 GB DDR memory.
Sound	Line In and Mic Out connectors.
Removable Hard Drive	3.5 in., ≥80 GB Serial ATA, 7200 RPM.
Optical Drive	Internal 4.7 GB DVD±R/RW.
External Display Port Type	One (1) DVI-D (primary - digital only) and one (1) DVI-I (secondary - digital and analog) connectors.
External Display Resolution	Up to 1600×1200 noninterlaced at 32 bit color, each for both primary and secondary displays.
Network Port	One (1) 10/100/1000 LAN with RJ-45 connector.
USB 2.0 Port	Seven (7); three (3) in front and four (4) in rear.

TLA7012 Integral Controls

Characteristic	Description
Front-panel Display	Size: 15 in. (38.1 cm) diagonal. Type: Active-matrix color TFT LCD with backlight. Resolution: 1024×768.
Simultaneous Display Capability	Both the front-panel and one external display can be used simultaneously at 1024×768 resolution.
Front-panel	General-purpose knob with dedicated hot-keys and knobs for horizontal and vertical scaling and scrolling.
Touchscreen	Available with Option 18.

TLA7PC1 Benchtop Controller Characteristics

Characteristic	Description
Operating System	Microsoft® Windows® XP Professional and Multilingual User Interface Pack.
Processor	3 GHz Intel® Pentium® 4.
Chipset	Intel® 945G.
Memory	1 GB dual channel DDR, PC 800 MHz (DIMM), expandable to 4 GB DDR memory.
Sound	Line In and Mic Out connectors.
Removable Hard Drive	3.5 in., 80 GB Serial ATA, 7200 RPM. Supports second Serial ATA Removable Hard Drive (includes second removable hard drive assembly only - user supplies second hard drive).
Optical Drive	Internal 4.7 GB DVD±R/RW.
External Display Port Type	One (1) analog DB-15 connector.
External Display Resolution	Up to 1600×1200 noninterlaced at 65,536 colors.
Network Port	One (1) 10/100/1000 LAN with RJ-45 connector.
USB 2.0 Port	Six (6); two (2) in front and four (4) in rear.
PS/2 Ports	Three (3); one (1) in front and two (2) in rear.
Enhanced Parallel Port	Standard DB25 female connector; supports EPP/SPP/ECP.
Serial Port	Standard DB9 male connector.
PCI Bus	Three full-size PCI slots, 32 bit, 33 MHz. Can be used to add up to three additional optional PCI Video Display cards, available from third-parties, for a total of four displays.

Integrated View (iView™) Capability

Characteristic	Description
TLA Mainframe Configuration Requirements	GPIB-iView (Opt. 1C) requires TLA Application Software 5.0 or greater.
Number of Tektronix oscilloscopes that can be connected to a TLA system	1
External Oscilloscopes Supported	More than 100. For a complete listing of currently supported oscilloscopes, please visit our website http://www.tektronix.com/iview.
TLA Connections	USB, Trigger In, Trigger Out, Clock Out.
Oscilloscope Connections	GPIB, Trigger In, Trigger Out, Clock In (when available) for the GPIB-iView cable (Opt. 1C).
Setup	iView™ external oscilloscope wizard automates setup.
Data Correlation	After oscilloscope acquisition is complete, the data is automatically transferred to the TLA and time correlated with the TLA acquisition data.
Deskew	The oscilloscope and TLA data is automatically deskewed and time correlated when using the iView™ external oscilloscope cable.
iView™ External Oscilloscope Cable Length	2 m

Symbolic Support

Characteristic	Description
Number of Symbols/Ranges	Unlimited (limited only by amount of virtual memory available on TLA).
Object File Formats Supported	IEEE695, OMF 51, OMF 86, OMF 166, OMF 286, OMF 386, COFF, Elf/Dwarf 1 and 2, Elf/Stabs, TSF (if your software development tools do not generate output in one of the above formats, TSF or the Tektronix symbol file, a generic ASCII file format is supported. The generic ASCII file format is documented in the TLA User Manual). If a format is not listed, please contact your local Tektronix representative.

TLA7012 and TLA7016 External Instrumentation Interfaces

Characteristic	Description
System Trigger Output	Asserted whenever a system trigger occurs (TTL-compatible output, back-terminated into 50 Ω).
System Trigger Input	Forces a system trigger (triggers all modules) when asserted (adjustable threshold between 0.5 V and 1.5 V, edge-sensitive, falling-edge latched).
External Signal Output	Can be used to drive external circuitry from a module's trigger mechanism (TTL-compatible output, back-terminated into 50 Ω).
External Signal Input	Can be used to provide an external signal to arm or trigger any or all modules (adjustable threshold between 0.5 V and 1.5 V, level-sensitive).

Power

Product	Characteristics
TLA7012	Voltage range/frequency: 90-250 VAC at 45-66 Hz. 100-132 VAC at 360-440 Hz. Input current: 7 A maximum at 90 VAC (70 A surge). Power consumption: 750 W maximum.
TLA7016	Voltage range/frequency: 90-250 VAC at 45-66 Hz, 100-132 VAC at 360-440 Hz. Input current: 16.5 A maximum at 90 VAC (70 A surge). Power consumption: 1,450 W maximum.
TLA7PC1	Voltage range/frequency: 100-240 VAC at 50-60 Hz. Input current: 3 A maximum at 100 VAC. Power consumption: 300 W maximum.
TL708EX	Voltage range/frequency: 100-240 VAC at 50-60 Hz. Input current: 2 A maximum at 100 VAC. Power consumption: 200 W maximum.

Environmental

Characteristic	Description
Temperature	Operating: +5 °C to +45 °C. Nonoperating: -20 °C to +60 °C.
Humidity	20% to 80%. Operating: ≤30 °C; 80% relative humidity (29 °C maximum wet-bulb temperature). Nonoperating: 8% to 80% (29 °C maximum wet-bulb temperature).
Altitude	Operating: -1,000 ft. to 10,000 ft. (-305 meters to 3,050 meters).
Safety	UL3111-1, CSA1010.1, EN61010-1, IEC61010-1.

Physical Characteristics

TLA7012 Portable

Dimensions	mm	in.
Height	295	11.6
Width	451	17.75
Depth	460	18.1
Weight	**kg**	**lb.**
Net (w/o modules)	14	30
Shipping (typical)	27	59

TLA7016 Benchtop

Dimensions	mm	in.
Height	350	13.7
Width	425	16.7
Depth	673	26.5
Weight	**kg**	**lb.**
Net (w/o modules)	25	55
Shipping (typical)	51.8	115

TLA7PC1 Benchtop Controller

Dimensions	mm	in.
Height	89	3.5
Width	432	17
Depth	483	19
Weight	**kg**	**lb.**
Net	9	19
Shipping	15	33

TL708EX 8-port Instrument Hub and Expander

Dimensions	mm	in.
Height	51	2
Width	445	17.5
Depth	305	12
Weight	**kg**	**lb.**
Net	3	6
Shipping	5	11

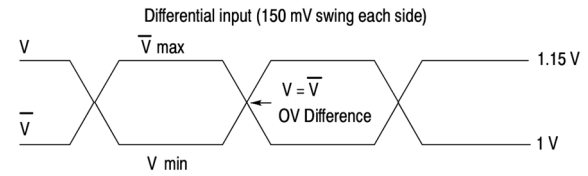
TLA7ACx Characteristics

General

Characteristic	Description
Number of Channels (all channels are acquired including clocks)	
TLA7AC2	68 channels (4 are clock channels).
TLA7AC3	102 channels (4 are clock and 2 are qualifier channels).
TLA7AC4	136 channels (4 are clock and 4 are qualifier channels).
Channel Grouping	No limit to number of groups or number of channels per group (all channels can be reused in multiple groups).
Module "Merging"	Up to five 102 channel or 136 channel modules can be "merged" to make up to a 680 channel module. Merged modules exhibit the same depth as the lesser of the five individual modules. Word/setup-and-hold/glitch/transition recognizers span all five modules. Range recognizers limited to three module merge. Only one set of clock connections is required.
Time Stamp	51 bits at 125 ps resolution (3.25 days duration).
Clocking/Acquisition Modes	Asynchronous/Synchronous 8 GHz MagniVu high-speed timing is available simultaneous with all modes.
Number of Mainframe Instrument Slots Required per TLA Series Module	1

Input Characteristics (with P68xx or P69xx probes)

Characteristic	Description
Capacitive Loading	0.5 pF clock/data (P69xx). <0.7 pF clock/data (P68xx). (1.0 pF for P6810 in group configuration).
Threshold Selection Range	From -2.0 V to +4.5 V in 5 mV increments. Threshold presets include TTL (1.5 V), CMOS (1.65 V), ECL (-1.3 V). PECL (3.7 V), LVPECL (2.0 V), LVCMOS 1.5 V (0.75 V), LVCMOS 1.8 V (0.9 V), LVCMOS 2.5 V (1.25 V), LVCMOS 3.3 V (1.65 V), LVDS (0 V), and user defined.
Threshold Selection Channel Granularity	Separate selection for each of the clock/qualifier channels and one per group of 16 data channels for each 34-channel probe.
Threshold Accuracy (including probe)	±(35 mV + 1%)
Input Voltage Range	
Operating	-2.5 V to 5.0 V
Nondestructive	±15 V
Minimum Input Signal Swing	300 mV (single ended). $V_{MAX} - V_{MIN} > 150$ mV (differential).
Input Signal Minimum Slew Rate	200 mV/ns typical.



Differential equivalent signal input (300 mV swing) as viewed by the logic analyzer and the analog probe output**.

* Note: For differential inputs, the module threshold should be set to OV (assuming no common mode error).

** Note: See online help for further analog output details.

State Acquisition Characteristics (with P68xx or P69xx probes)

Full Channel	Half Channel	Quarter Channel
235 MHz	450 MHz / 450 Mb/s or 470 Mb/s (DDR)	450 MHz / 900 Mb/s
450 MHz Optional	800 MHz / 800 Mb/s or 900 Mb/s (DDR)	625 MHz / 1.25 Gb/s

Characteristic	Description
State Record Length with Time Stamps	(quarter/half/full channels) 8/4/2 Mb, 32/16/8 Mb, 128/64/32 Mb, 512/256/128 Mb per channel.
Setup-and-Hold Time Selection Range	From 16 ns before, to 8 ns after clock edge in 125 ps increments. Range may be shifted towards the setup region by 0 ns [+8, -8] ns, 4 ns [+12, -4] ns, or 8 ns [+16, 0] ns.
Setup-and-Hold Window	
All Channels	625 ps typical.
Single Channel	500 ps typical.
Minimum Clock Pulse Width	500 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880), 700 ps (P6810).
Active Clock Edge Separation	400 ps.
Demux Channel Selection	Channels can be demultiplexed to other channels through user interface with 8-channel granularity.
Source Synchronous Clocking	Up to four "Fast Latches" per module (20 max per 5-way merge) to strobe source-synchronous buses into TLA7ACx Modules. Four sets of any predefined "Fast Latches" may be combined with qualification data and data pipelining to store four independent source-synchronous data buses. Two "Fast Latches" may be combined to address DDR applications.

Timing Acquisition Characteristics (with P68xx or P69xx probes)

Characteristic	Description
MagniVu™ Timing	125 ps max, adjustments to 250 ps, 500 ps, 1 ns, and 2 ns.
MagniVu Timing Record Length	16 kb per channel, with adjustable trigger position.
Deep Timing Resolution (quarter/half/full channels)	500 ps/1 ns/2 ns to 50 ms.
Deep Timing Resolution with Glitch Storage Enabled	4 ns to 50 ms.
Deep Timing Record Length (quarter/half/full channels with time stamps and with or without transitional storage)	8/4/2 Mb, 32/16/8 Mb,128/64/32 Mb, 512/256/128 Mb per channel.
Deep Timing Record Length with Glitch Storage Enabled	Half of default main memory depth.
Channel-to-channel Skew	300 ps typical.
Minimum Recognizable Pulse/Glitch Width (single channel)	500 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880), 750 ps (P6810).
Minimum Detectable Setup/Hold Violation	250 ps
Minimum Recognizable Multichannel Trigger Event	Sample period + channel-to-channel skew.

Analog Acquisition Characteristics (with P68xx or P69xx probes)

Characteristic	Description
Bandwidth	2 GHz typical.
Attenuation	10x, ±1%.
Offset and Gain (Accuracy)	±50 mV, ±2% of Signal Amplitude.
Channels Demultiplexed	4
Run/Stop Requirements	None, analog outputs are always active.
iCapture™ Analog Outputs	Compatible with any supported Tektronix oscilloscope.
iCapture Analog Output BNC Cable	Low loss, 10x, 36 in. Basic Analog Multiplexer functionality is offered standard on all TLA7ACx modules. This routes 4 fixed channels to the iCapture Analog Output BNCs. The outputs can not be switched to other logic analyzer channels. Option AM enables full analog multiplexer control and allows the routing of any 4 logic analyzer channels to the iCapture Analog Output BNCs.

Trigger Characteristics

Characteristic	Description
Independent Trigger States	16
Maximum Independent If/Then Clauses per State	16
Maximum Number of Events per If/Then Clause	8
Maximum Number of Actions per If/Then Clause	8
Maximum Number of Trigger Events	18 (2 counter/timers plus any 16 other resources)
Number of Word Recognizers	16
Number of Transition Recognizers	16
Number of Range Recognizers	4
Number of Counter/Timers	2
Trigger Event Types	Word, group, channel, transition, range, anything, counter value, timer value, signal, glitch, setup-and-hold violation, snapshot.
Trigger Action Types	Trigger module, trigger all modules, trigger main, trigger MagniVu, store, don't store, store sample, increment counter, decrement counter, reset counter, start timer, stop timer, reset timer, snapshot current sample, goto state, set/clear signal, do nothing.
Maximum Triggerable Data Rate	1250 Mb/s (4X clocking mode).
Trigger Sequence Rate	DC to 500 MHz (2 ns).
Counter/Timer Range	51 bits each (>50 days at 2 ns).
Counter Rate	DC to 500 MHz (2 ns).
Timer Clock Rate	500 MHz (2 ns).
Counter/Timer Latency	2 ns.
Range Recognizers	Double bounded (can be as wide as any group (408 channel max), must be grouped according to specified order of significance).
Setup-and-Hold Violation Recognizer Setup Time Range	From 8 ns before to 7 ns after clock edge in 125 ps increments. This range may be shifted towards the positive region by 0 ns, 4 ns, or 8 ns.
Setup-and-Hold Violation Recognizer Hold Time Range	From 7 ns before to 8 ns after clock edge in 125 ps increments. This range may be shifted towards the positive region by 0 ns [+8, –8] ns, 4 ns [+12, –4] ns, or 8 ns [+16, 0] ns.
Trigger Position	Any data sample.
MagniVu Trigger Position	MagniVu position can be set from 0% to 60% centered around the MagniVu trigger.
Storage Control (data qualification)	Global (conditional), by state (start/stop), block, by trigger action, or transitional. Also force main prefill selection available.

Physical Characteristics

Dimensions	mm	in.
Height	262	10.3
Width	61	2.4
Depth	381	15
Weight	**kg**	**lb.**
Net	3.1	6.7
Shipping	6.3	13.7

TLA7Bxx Characteristics

General

Characteristic	Description
Number of Channels (all channels are acquired including clocks)	
TLA7BB2	68 channels (4 are clock channels)
TLA7BB3	102 channels (4 are clock, 2 are qualifier channels)
TLA7BB4	136 channels (4 are clock, 4 are qualifier channels)
TLA7BC4	136 channels (4 are clock, 4 are qualifier channels) (128 Mb)
Channel Grouping	No limit to number of groups or number of channels per group (all channels can be reused in multiple groups).
Module "Merging"	Up to five 68 channel, 102 channel, or 136 channel modules can be "merged" to make up to a 680 channel module. Merged modules exhibit the same depth as the lesser of the five individual modules. Word/setup-and-hold/glitch/transition recognizers span all five modules. Range recognizers limited to three module merge. Only one set of clock connections is required.
Time Stamp	54 bits at 20 ps resolution (>4 days duration)
Clocking/Acquisition Modes	Asynchronous and Synchronous. 20 ps (50 GHz) MagniVu, high-speed timing is available simultaneous with all modes.
Number of Mainframe Instrument Slots Required per TLA Series Module	1

Input Characteristics (with P68xx or P69xx probes)

Characteristic	Description
Capacitive Loading	0.5 pF clock/data (P69xx)
	<0.7 pF clock/data (P68xx); 1.0 pF for P6810 when 8-channel podlet grouper is used
Threshold Selection Range	From -2.0 V to +4.5 V in 5 mV increments. Threshold presets include TTL (1.5 V), CMOS (2.5 V), ECL (-1.3 V), PECL (3.7 V), LVPECL (2.0 V), LVCMOS 1.5 V (0.75 V), LVCMOS 1.8 V (0.9 V), LVCMOS 2.5 V (1.25 V), LVCMOS 3.3 V (1.65 V), LVDS (0 V), and user defined
Threshold Selection Channel Granularity	Separate selection for each of the clock/qualifier and individual channels
Threshold Accuracy (including probe)	±(35 mV + 1%)
Input Voltage Range	
Operating	-2.5 V to 5.0 V
Nondestructive	±15 V
Minimum Input Signal Swing	200 mV (single ended)
	V_{MAX} - V_{MIN} > 100 mV (differential)
Input Signal Minimum Slew Rate	200 mV/ns typical

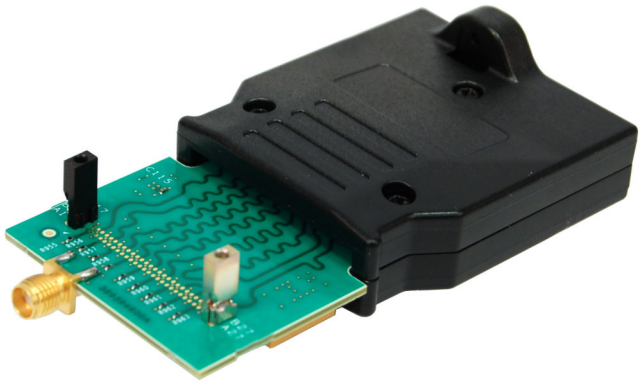
State Acquisition Characteristics (with P68xx or P69xx probes)

Configuration	Full Channel	Half Channel
750 MHz Standard	750 MHz / 750 Mb/s (1 sample/clock) 750 MHz / 1.5 Gb/s (2 samples/clock)	750 MHz / 3 Gb/s (4 samples/clock)
1.4 GHz Optional	1.4 GHz / 1.4 Gb/s (1 sample/clock)	1.4 GHz / 2.8 Gb/s (2 samples/clock)

Characteristic	Description
State Record Length with Time Stamps (half/full channels)	4/2 Mb, 8/4 Mb, 16/8 Mb, 32/16 Mb, 64/32 Mb, 128/64 Mb per channel, 256/128 Mb per channel (TLA7BC4)
Setup-and-Hold Time Selection Range	From 15 ns before, to 7.5 ns after clock edge in 20 ps increments. Range may be shifted towards the setup region by 0 ns [+7.5, -7.5] ns, 2.5 ns [+10, -5] ns, or 7.5 ns [+15, 0] ns
Setup-and-Hold Window, Single Channel	180 ps typical
Minimum Clock Pulse Width	200 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880), 250 ps (P6810)
Demux Channel Selection	Channels can be demultiplexed to other channels through user interface with 8-channel granularity

Timing Acquisition Characteristics (with P68xx or P69xx probes)

Characteristic	Description
MagniVu™ Timing	20 ps max, adjustments to 40 ps, 80 ps, 160 ps, 320 ps, and 640 ps
MagniVu Timing Record Length	128 kb per channel, with adjustable trigger position
Deep Timing Resolution (quarter/half/full channels)	156.25 ps/312.5 ps/625 ps to 50 ms
Deep Timing Resolution with Glitch Storage Enabled	1.25 ns to 50 ms
Deep Timing Record Length (quarter/half/full channels)	8/4/2 Mb, 16/8/4 Mb, 32/16/8 Mb, 64/32/16 Mb, 128/64/32 Mb, 256/128/64 Mb per channel; 512/256/128 (TLA7BC4)
Deep Timing Record Length with Glitch Storage Enabled	Half of default main memory depth
Channel-to-Channel Skew (module + probes)	
Before Customer Deskew	±80 ps typical
After Customer Deskew *(See AutoDeskew information below)*	±20 ps typical
Minimum Recognizable Pulse/Glitch Width (single channel)	200 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880) 250 ps (P6810)
Minimum Detectable Setup/Hold Violation	40 ps
Minimum Recognizable Multichannel Trigger Event	Sample period + channel-to-channel skew



AutoDeskew and Customer Deskew Fixture

Tektronix recommends **AutoDeskew**, a standard feature available within the TLA Application, for deskewing probe channels and setting the sample point for synchronous applications. However, for tight time alignment in both synchronous and asynchronous applications (including MagniVu), Tektronix recommends the **Customer Deskew Fixture**. This is an optional accessory to the TLA7Bxx modules that is used to perform a "channel-to-channel deskew" of the probes connected to the TLA7Bxx module to ensure tight time alignment between all channels across all probes. Two different fixtures are available:

- Customer Deskew Fixture for P6800 Series Probes
- Customer Deskew Fixture for P6900 Series Probes

For ordering details, please see the Ordering Information section.

Analog Acquisition Characteristics (with P68xx or P69xx probes)

Characteristic	Description
Bandwidth	3 GHz (typical)
Attenuation	10x, ±1%
Offset and Gain (Accuracy)	±50 mV, ±2% of Signal Amplitude
Channels Demultiplexed	4
Run/Stop Requirements	None, analog outputs are always active
iView™ Analog Outputs	Compatible with any supported external Tektronix oscilloscope
iView Analog Output BNC Cables	Four (4) low loss, 10x, 36 in.

Physical Characteristics

Dimensions	mm	in.
Height	262	10.3
Width	61	2.4
Depth	381	15
Weight	**kg**	**lb.**
Net	3.1	6.7
Shipping	6.3	13.7

Trigger Characteristics

Characteristic	Description
Independent Trigger States	16
Maximum Independent If/Then Clauses per State	16
Maximum Number of Events per If/Then Clause	8
Maximum Number of Actions per If/Then Clause	8
Maximum Number of Trigger Events	26 (2 counter/timers plus any 24 other resources)
Number of Word Recognizers	24
Number of Transition Recognizers	24
Number of Range Recognizers	8
Number of Counter/Timers	2
Trigger Event Types	Word, group, channel, transition, range, anything, counter value, timer value, signal, glitch, setup-and-hold violation, snapshot
Trigger Action Types	Trigger module, trigger all modules, trigger main, trigger MagniVu, store, don't store, start store, stop store, increment counter, decrement counter, reset counter, start timer, stop timer, reset timer, snapshot current sample, goto state, set/clear signal, do nothing
Maximum Triggerable Data Rate	3.0 Gb/s
Trigger Sequence Rate	DC to 800 MHz (1.25 ns)
Counter/Timer Range	48 bits each (~4 days at 1.25 ns)
Counter Rate	DC to 800 MHz (1.25 ns)
Timer Clock Rate	800 MHz (1.25 ns)
Counter/Timer Test Latency	0 ns
Range Recognizers	Double bounded (can be as wide as any group (408 channel max), must be grouped according to specified order of significance)
Setup-and-Hold Violation Recognizer	
Setup Time Range	From 7.5 ns before to 7.5 ns after clock edge in 20 ps increments. This range may be shifted towards the positive region by 0 ns, 2.5 ns, 5 ns, or 7.5 ns.
Hold Time Range	
Trigger Position	Any data sample
MagniVu Trigger Position	MagniVu position can be set from 0% to 60% centered around the MagniVu trigger
Storage Control (data qualification)	All, Global (conditional), by state (start/stop), block, by trigger action, or transitional. Also force main prefill selection available.

P68xx/69xx Probe Characteristics

	P6810	P6860	P6864	P6880	P6960	P6962/P6964	P6962DBL	P6980	P6982
Data	Differential	Single-ended	Single-ended	Differential	Single-ended	Single-ended	Single-ended	Differential	Differential
Clock	Differential								
Number of Channels	34	34	17	34	34	34	34	34	17
Number of Probe Heads	1	2	1	4	1	1	1	2	1
Recommended Use	General-purpose applications.	Good signal density and quick reliable attachment.	Data rates in excess of 750 MHz (TLA7Bxx) or 450 MHz (TLA7ACx) with good signal density.	Full differential probing with good signal density.	Best signal density and quick reliable attachment. Flying leads for general-purpose probing is optional.	Data rates in excess of 750 MHz (TLA7Bxx) or 450 MHz (TLA7ACx) with the best signal density.	Highest performance applications, such as the fastest data rate DDR memory.	Full differential probing with the best signal density.	Full differential with the best signal density for data rates in excess of 750 MHz (TLA7Bxx) or 450 MHz (TLA7ACx).
Attachment to Target System	Fits both 0.100 inch and 2 mm square pin configurations	Compression Elastomer			D-Max® probing technology compression cLGA				
Probe Loading AC/DC	< 0.7 pF/20 kΩ to Ground				0.5 pF/20 kΩto Ground, typical		0.7 pF/11.7 kΩ to Ground, typical	0.5 pF/20 kΩto Ground, typical	
Analog Bandwidth	Module Dependent								
TLA7Bxx module	3 GHz through iCapture™ to analog out BNCs*1								
TLA7ACx module	2 GHz through iCapture™ to analog out BNCs*1								
Input Range	-2.5 V to 5.0 V						-1.25 V to +2.5 V	-2.5 V to 5.0 V	
Max Voltage (nondestruct)	±15 V						±7.5 V	±15 V	
Cable Length	1.8 m (6 ft.)								

*1 Analog bandwidth of P6960 is less with flying lead set attached.

TLA7Sxx Characteristics

General

Characteristic	Description
Number of Channels	
TLA7S08	8 channels
TLA7S16	16 channels
Record Length	32M 8b/10b symbols per channel
Time Stamp Range	62 hours
Time Stamp	54 bits at 25 ps resolution
Clocking/Acquisition Modes	TLA Module without SSC (Spread Spectrum Clocking) , External Reference Clock (100 Mhz ±10% or 125 Mhz) with or without SSC
External Reference Clock Frequency Tolerance	±350 ppm
Number of Mainframe Instrument Slots Required per TLA Series Module	1

Module Configuration Requirements

Module	Bi-Directional Link Width			
	x1	x4	x8	x16
TLA7S08	1	1	0	0
TLA7S16	1	1	1	2

Input Characteristics (with P67xx probes)

Characteristic	Description
Capacitive Loading	See P67xx Probe Manual
Minimum data eye	See P67xx Probe Manual

Acquisition Characteristics (with P67xx probes)

Characteristic	Description
Dynamic link-width switch latency	Consumes up to 48 symbols (typical)
FTS support	Consumes up to 12 FTS packets (typical)

Filter Characteristics

Characteristic	Description
Ordered Sets	TS1, TS2, SKP, EIOS, FTS, EIEOS
DLLPs	Ack, Nak, PM, Vendor Specific, InitFC1, InitiFC2, UpdateFC
TLPs	MRd, MRdL, MWr, IORd, IOWr, CfgRd0, CfgWr0, CfgRd1, CfgWr1, Msg, MsgD, Cpl, CplD, CPlLk, CPlDLk

Trigger Characteristics

Characteristic	Description
Independent Trigger States	8
Maximum Independent If/Then Clauses per State	8
Maximum Number of Events per If/Then Clause	8
Maximum Number of Actions per If/Then Clause	8
Maximum Number of Event Counters per State	2
Event Counter Range	16 bit
Number of TLP Packet Recognizers per link direction	4
Number of DLLP Packet Recognizers per link direction	4
Number of Sequence Recognizers	4
Number of Symbols per Sequence Recognizer	16
Number of Link Event Recognizers	4
Number of Global Counter/Timers	4
Trigger Event Types	Anything, TLP, DLLP, sequence, link event, counter, timer
Trigger Action Types	Trigger, trigger all modules, wait for system trigger, goto, increment counter, decrement counter, reset counter, start timer, reset timer, reset and start timer, stop timer, reset and stop timer, set signal out, clear signal out, arm module, start storage, stop storage, do nothing
Counter/Timer Range	48 bit (~5 days with 3.6 ns resolution)
Storage Control (data qualification)	by State (Start/Stop)

Physical Characteristics

	TLA7S16		TLA7S08	
Dimensions	**mm**	**in.**	**mm**	**in.**
Height	262	10.3	262	10.3
Width	61	2.4	61	2.4
Depth	381	15	381	15
Weight	**kg**	**lb.**	**kg**	**lb.**
Net	2.45	5.40	2.345	5.17
Shipping	6.505	14.34	6.445	14.21

P67xx Probe Characteristics

General

Characteristic	P6708	P6716	P6701S	P6704S	P6708S	P6716S	P6701SD
Probe Type	PCI Express Mid-bus Differential Data	PCI Express Mid-bus Differential Data	PCI Express Slot Interposer	PCI Express Slot Interposer	PCI Express Slot Interposer	PCI Express Slot Interposer	PCI Express Differential Solder-down Probe
Number of Channels	8	16	2	4	16	32	1
Recommended Use	Recommended where signal integrity is critical.	Recommended where signal integrity is critical.	Recommended for platforms with no mid-bus footprints and the PCI Express slot is the only probe access point.	Recommended for platforms with no mid-bus footprints and the PCI Express slot is the only probe access point.	Recommended for platforms with no mid-bus footprints and the PCI Express slot is the only probe access point.	Recommended for platforms with no mid-bus footprints and the PCI Express slot is the only probe access point.	Recommended for platforms with no mid-bus footprint, PCI Express slot; or where space is limited.
Attachment to Target System	Compression cSpring	Compression cSpring	PCI Express Slot	PCI Express Slot	PCI Express Slot	PCI Express Slot	Solder Down
Probe Loading AC/DC	See TLA P67xx and P67xxS Probe Manual						
Cable Length	1.8 m (6 ft.)						

Mid-bus Probe Configuration

x1	x4	x8	x16
1 P6708 1 TLA7S08	1 P6708 1 TLA7S08	-	-
1 P6716 1 TLA7S08	1 P6716 1 TLA7S08	-	-
1 P6708 1 TLA7S16	1 P6708 1 TLA7S16	2 P6708 1 TLA7S16	-
1 P6716 1 TLA7S16	1 P6716 1 TLA7S16	1 P6716 1 TLA7S16	2 P6716 2 TLA7S16

Slot Interposer Probe Configurations

x1	x4	x8	x16
1 P6701S 1 TLA7S08	-	-	-
1 P6704S 1 TLA7S08	1 P6704S 1 TLA7S08	-	-
1 P6708S 1 TLA7S16	1 P6708S 1 TLA7S16	1 P6708S 1 TLA7S16	-
1 P6716S 1 TLA7S16	1 P6716S 1 TLA7S16	1 P6716S 1 TLA7S16	1 P6716S 2 TLA7S16

Solder Down Application

Solder Down Probe Configurations

x1	x4	x8	x16
2 P6701SD 1 TLA7S08	8 P6704S 1 TLA7S08	–	–
2 P6701SD 1 TLA7S16	8 P6704S 1 TLA7S16	16 P6704S 1 TLA7S16	32 P6701SD 2 TLA7S16

Parameter		Description*2
Mid-bus probe	Minimum eye height at footprint pad*2	30 mV (single ended)
	Minimum eye width at footprint pad	0.53 UI if jitter frequency components of ≤40 MHz are not present.*3 If jitter frequency components of ≤40 MHz are present, then apply the filter function described in the graph to the jitter of the signal. (See user manual Figure 36)
Solder-down probe	Minimum eye height at footprint pad*2	30 mV (single ended)
	Minimum eye width at footprint pad	0.53 UI if jitter frequency components of ≤40 MHz are not present.*3 If jitter frequency components of ≤40 MHz are present, then apply the filter function described in the graph to the jitter of the signal. (See user manual Figure 36)
Slot interposer	Minimum eye height at probe connection point*2	60 mV (single ended)
	Minimum eye width at probe connection point	0.58 UI if jitter frequency components of ≤40 MHz are not present.*3 If jitter frequency components of ≤40 MHz are present, then apply the filter function described in the graph to the jitter of the signal. (See user manual Figure 36)
Unit Interval Gen1		400 ps
Unit Interval Gen2		200 ps

*2 Eye Height/Width values apply to both data rates.

*3 Requirements valid for 10^{-12} BER. Refer to the user manual for further information.

Ordering Information

TLA7012

Portable Logic Analyzer Mainframe, holds two TLA modules.

Includes: Mini Keyboard (119-7275-xx), Optical Wheel Mouse (119-7054-xx), Front-panel cover (200-4939-xx), One dual-wide panel filler for empty slots (333-4206-xx), TLA Application Software CD (063-3881-xx), Certificate of Traceable Calibration.
Please specify power cord, language, and service options when ordering.

TLA7012 Options

Option	Description	Order Number
Opt. 18	Add touchscreen	N/A
Opt. 1C	Add iView™ external oscilloscope interface kit	012-1614-xx
Opt. PO	Add Accessory Pouch for TLA7012	016-1441-xx
Opt. TL	Add Teklink Cable	174-5019-xx
Opt. 1K	Add LACART logic analyzer cart	LACART
Opt. 88	Factory install of module	N/A

TLA7012 Optional Accessories

Order Number	Accessory
650-4815-xx	Additional Removable Hard Drive Assembly (no SW)
020-2664-xx	Rackmount Kit
016-1522-xx	Wheeled Transport Case

TLA7016

Benchtop Logic Analyzer Mainframe, holds six TLA modules.

Includes: Five (5) dual-wide panel fillers for empty slots (333-4206-xx), LAN cable, straight-through, RJ-45 (174-5225-xx), TLA Application Software CD (063-3881-xx), Certificate of Traceable Calibration.
Please specify power cord, language, and service options when ordering.

TLA7016 Options

Option	Description	Order Number
Opt. 1C	Add iView™ external oscilloscope interface kit	012-1614-xx
Opt. TL	Add Teklink Cable	174-5019-xx
Opt. BTB	Add Benchtop System Mounting Brackets	407-5127-xx (Left) 407-5132-xx (Right)
Opt. 1K	Add K4000 logic analyzer cart	K4000
Opt. 88	Factory install of module	N/A

TLA7016 Optional Accessories

Order Number	Accessory
020-2369-xx	Rackmount Kit
016-1651-xx	Wheeled Transport Case

TLA7PC1

Controller for TLA7016 Benchtop Logic Analyzer Mainframe.

Includes: Mini USB keyboard (119-7275-xx), Optical Wheel Mouse (119-7054-xx), LAN cable, straighthrough, RJ-45 (174-5225-xx), TLA Application Software CD (063-3881-xx) (no recovery media).
Please specify power cord, language, and service options when ordering.

TL708EX

TekLink™ 8-port Instrument Hub and Expander (Used for connecting 3-to-8 TLA7012 or TLA7016 mainframes).

Includes: Instruction sheet (071-1765-xx, English only).
Please specify power cord and service options when ordering.

TLA7000 Series Power Cord Options

Option	Description	Order Number
Opt. A0	North America power	TLA7012/TLA7PC1/TL708EX: 161-0104-00 TLA7016: 161-0213-00 [15A], 161-0218-00 [20A]
Opt. A1	Universal EURO power	TLA7012/TLA7PC1/TL708EX: 161-0104-06 TLA7016: 161-0209-00
Opt. A2	United Kingdom power	TLA7012/TLA7PC1/TL708EX: 161-0104-07 TLA7016: 161-0210-00
Opt. A3	Australia power	TLA7012/TLA7PC1/TL708EX: 161-0104-14 TLA7016: 161-0211-00
Opt. A4	240 V, North America power	TLA7012/TLA7PC1/TL708EX: 161-0104-08 TLA7016: 161-0208-00
Opt. A5	Switzerland power	TLA7012/TLA7PC1/TL708EX: 161-0167-00 TLA7016: 161-0212-00
Opt. A6	Japan power	TLA7012/TLA7PC1/TL708EX: 161-A005-00 TLA7016: 161-0218-00
Opt. A10	China power	TLA7012/TLA7PC1/TL708EX: 161-0306-00 TLA7016: 161-0320-00
Opt. A11	India power	TLA7012/TLA7PC1/TL708EX: 161-0324-xx TLA7016: 161-0338-xx
Opt. A99	No power cord or AC adapter	–

TLA7000 Series Language Options

Option	Description
Opt. L0	English Manuals
Opt. L5	Japanese Manuals
Opt. L10	Russian Manuals
Opt. L99	No Manuals

TLA7000 Series Installation Service

Option	Description
LAINSTAL-SM	Installation of single mainframe and up to 3 modules or 1 to 3 modules in existing mainframe
LAINSTAL-LG	Installation of single mainframe and 4 to 6 modules

Gigabit LAN (GbE) Switch

Order Number	Description
020-2666-xx	16-port Gigabit LAN (GbE) Switch with U.S. Standard (120 V, 60 Hz) Power Cord

Power Cords for Gigabit LAN (GbE) Switch

Order Number	Description
161-0066-00	Power Cord, IEC320 C13, North American, Straight
161-0066-09	Power Cord, IEC320 C13, Universal Euro, Straight
161-0066-10	Power Cord, IEC320 C13, Universal Euro, Straight
161-0066-11	Power Cord, IEC320 C13, Australian, Straight
161-0066-12	Power Cord, IEC320 C13, North American, Straight
161-0154-00	Power Cord, IEC320 C13, Switzerland, Straight
161-0298-00	Power Cord, IEC320 C13, Japan, Straight
161-0304-00	Power Cord, IEC320 C13, China, Straight

TLA7ACx Modules

Includes: Certificate of calibration, and one-year warranty (return to Tektronix). Probes must be ordered separately.

TLA7ACx Logic Analyzer Modules

Module	Description
TLA7AC2	68-channel Logic Analyzer module, 8 GHz timing, 235 MHz state, 2 Mb record length. Options for up to 128 Mb record length and/or up to 450 MHz state.
TLA7AC3	102-channel Logic Analyzer module, 8 GHz timing, 235 MHz state, 2 Mb record length. Options for up to 128 Mb record length and/or up to 450 MHz state.
TLA7AC4	136-channel Logic Analyzer module, 8 GHz timing, 235 MHz state, 2 Mb record length. Options for up to 128 Mb record length and/or up to 450 MHz state.

TLA7ACx Module Options

Base configuration is 2 Mb record length at 235 MHz state with basic Analog Multiplexer capability.

Option	Description
Opt. 1S	Increase to 8 Mb Record Length at 235 MHz State.
Opt. 2S	Increase to 32 Mb Record Length at 235 MHz State.
Opt. 3S	Increase to 128 Mb Record Length at 235 MHz State.
Opt. 4S	Increase to 2 Mb Record Length at 450 MHz State.
Opt. 5S	Increase to 8 Mb Record Length at 450 MHz State.
Opt. 6S	Increase to 32 Mb Record Length at 450 MHz State.
Opt. 7S	Increase to 128 Mb Record Length at 450 MHz State.
Opt. AM	Enable Full Analog Multiplexer.
Opt. 88	Factory Install

TLA7ACx Language Options

Option	Description
Opt. LG1	Global Manuals
Opt. L99	No Manuals

Please refer to the Service section at the rear of this document for details about Calibration and Repair options.

TLA7Bxx Modules

Includes: Certificate of calibration, and one-year warranty (return to Tektronix).
Note: Probes must be ordered separately.

TLA7Bxx Logic Analyzer Modules

Module	Description
TLA7BB2	68-channel logic analyzer module, 50 GHz MagniVu timing, 750 MHz state clock, 2 Mb record length. Options for up to 64 Mb record length and/or up to 1.4 GHz state clock.
TLA7BB3	102-channel logic analyzer module, 50 GHz MagniVu timing, 750 MHz state clock, 2 Mb record length. Options for up to 64 Mb record length and/or up to 1.4 GHz state clock.
TLA7BB4	136-channel logic analyzer module, 50 GHz MagniVu timing, 750 MHz state clock, 2 Mb record length. Options for up to 64 Mb record length and/or up to 1.4 GHz state clock.
TLA7BC4	136 channel logic analyzer module, 50 GHz MagniVu timing, 750 MHz state clock, 128 Mb record length. Option for 1.4 GHz state clock.

TLA7Bxx Module Options

Base configuration is 2 Mb record length at 750 MHz state clock with full Analog Multiplexer capability.

Option	Description
Opt. 1S	Increase to 4 Mb Record Length at 750 MHz State Clock
Opt. 2S	Increase to 8 Mb Record Length at 750 MHz State Clock
Opt. 3S	Increase to 16 Mb Record Length at 750 MHz State Clock
Opt. 4S	Increase to 32 Mb Record Length at 750 MHz State Clock
Opt. 5S	Increase to 64 Mb Record Length at 750 MHz State Clock
Opt. 6S	Increase to 2 Mb Record Length at 1.4 GHz State Clock
Opt. 7S	Increase to 4 Mb Record Length at 1.4 GHz State Clock
Opt. 8S	Increase to 8 Mb Record Length at 1.4 GHz State Clock
Opt. 9S	Increase to 16 Mb Record Length at 1.4 GHz State Clock
Opt. AS	Increase to 32 Mb Record Length at 1.4 GHz State Clock
Opt. BS	Increase to 64 Mb Record Length at 1.4 GHz State Clock
Opt. 88	Factory Install

TLA7BC4 Module Options

Base configuration is 128 Mb record length at 750 MHz state clock.

Option	Description
Opt. 1S	Increase to 1.4 GHz State Clock

TLA Series Module Upgrades

Please refer to the Service section at the rear of this document for details about Calibration and Repair options.

TLA7Bxx Customer Deskew Fixture

Option	Description
020-2942-00	TLA7Bxx Customer Deskew Fixture for P6800 Series Probes
020-2940-00	TLA7Bxx Customer Deskew Fixture for P6900 Series Probes

TLA7Bxx Language Options

Option	Description
Opt. L0	English Manuals
Opt. L5	Japanese Manuals
Opt. L10	Russian Manuals
Opt. L99	No Manuals

TLA7Sxx PCI Express Modules

Includes: Statement of Compliance, one-year warranty (return to Tektronix), reference clock cable (672-6285-00), and reference clock jumper cable (174-5392-00).
Probes must be ordered separately.

Module	Description
TLA7S16	16-channel Serial Analyzer module, 2.5 Gb/s and 5.0 Gb/s acquisition, 32 MSymbol record length per channel.
TLA7S08	8-channel Serial Analyzer module, 2.5 Gb/s and 5.0 Gb/s acquisition, 32 MSymbol record length per channel.

Logic Analyzer TLA7Sxx Module Options

Option	Description
Opt. 88	Factory Install
Opt. L0	English Manual
Opt. L5	Japanese Manual
Opt. L10	Russian Manual
Opt. L99	No Manual

Service Options

Please refer to the rear of this document for information on Calibration and Repair options for these TLA modules.

Tektronix Logic Analyzer Probes

Models	Description
P6708	8-channel PCI Express Mid-bus Probe and Accessories **Includes**: Statement of Compliance, (2) 8-channel retention mechanisms, Velcro Cable Managers, Probe instruction manual.
P6716	16-channel PCI Express Mid-bus Probe and Accessories **Includes**: Statement of Compliance, (2) 16-channel retention mechanisms, Velcro Cable Managers, Probe instruction manual.
P6701S	x1 PCI Express Slot Interposer **Includes**: Statement of Compliance, Velcro Cable Managers, Probe instruction manual.
P6704S	x4 PCI Express Slot Interposer **Includes**: Statement of Compliance, Velcro Cable Managers, Probe instruction manual.
P6708S	x8 PCI Express Slot Interposer **Includes**: Statement of Compliance, Velcro Cable Managers, Probe instruction manual.
P6716S	x16 PCI Express Slot Interposer **Includes**: Statement of Compliance, Velcro Cable Managers, Probe instruction manual.
P6701SD	x1 PCI Express Differential Solder-down Probe **Includes**: Statement of Compliance, Velcro Cable Managers, Probe instruction manual.
P6810	34-channel General-purpose Probe with Differential Clock, Differential Data, and Accessories. Opt. DL: Differential flying lead set (196-3471-xx).
P6860	34-channel High-density Compression Probe, with Differential Clock, Single-ended Data, and Accessories.
P6864	17-channel (optimized for quarter-channel mode) High-density Compression Probe, with Differential Clock, Single-ended Data, and Accessories.
P6880	34-channel High-density Compression Probe with Differential Clock, Differential Data, and Accessories.
P6960	34-channel Single-ended High-density Compression Probe with D-Max™ Probing Technology, with Differential Clock, Single-ended Data, and Accessories. Opt 01: 34-channel general-purpose flying lead set (196-3494-xx).
P6962	34-channel (optimized for half-channel mode) Single-ended High-Density Compression Probe with D-Max® Probing Technology with Differential Clock, Single-ended Data and Accessories.
P6962DBL	34-channel (optimized for half-channel mode) Single-ended High-density Compression Probe with D-Max® Probing Technology with Differential Clock, Single-ended Data and Accessories.
P6964	34-channel (optimized for quarter-channel mode) Single-ended High-Density compression Probe with D-Max® Probing Technology with Differential Clock, Single-ended Data, and Accessories.
P6980	34-channel Differential High-density Compression Probe with D-Max® Probing Technology, with Differential Clock, Differential Data, and Accessories.
P6982	17-channel (optimized for half-channel mode) Differential High-density Compression Probe with D-Max® Probing Technology, with Differential Clock, Differential Data, and Accessories.

Language Options

Option	Description
Opt. L0	English Manuals
Opt. L99	No Manuals

Service Options

Please refer to the Service section at the rear of this document for information on Calibration and Repair options for these probes.

Probe Accessories

P67xx Mid-bus Standard Accessories

	P6708		P6716	
Description	**Qty Per Probe**	**Part Number**	**Qty Per Probe**	**Part Number**
Retention Mechanisms	2	020-2785-00	2	020-2784-00
Sheet of Probe Labels	1	335-1729-00	1	335-1728-00
Probe Adjustment Tool	1	003-1890-00	1	003-1890-00
Velcro Cable Manager (Bag of 2)	1	346-0300-00	1	346-0300-00

P6701SD Solder-down Standard Accessories

Description	Qty Per Probe	Part Number
TriMode™ Long Reach Solder Tip	1	P75TLRST
Storage Case	1	016-2009-00
Solder Tip Tape (Strip of 10)	1	006-8237-xx
1 - .004 wire / 1 - .008 wire / 1 - SAC305 Solder (Package of 3 bobbins)	1	020-2754-xx
Hook and Loop fastening straps and dots	1	016-1953-xx
Installation Sheet	1	071-2503-xx

P6701SD Solder-down Required Accessories

Description	Qty*[4]	Part Number
Power Adapter	1	870-0192-00

*[4] See Solder-down Probe Configuration for Required Quantities.

P6701SD Solder-down Optional Accessories

Description	Qty	Part Number
Bullet Removal Tool	1	003-1896-xx
Replacement bullet contacts	Pack of 4	003-0359-xx

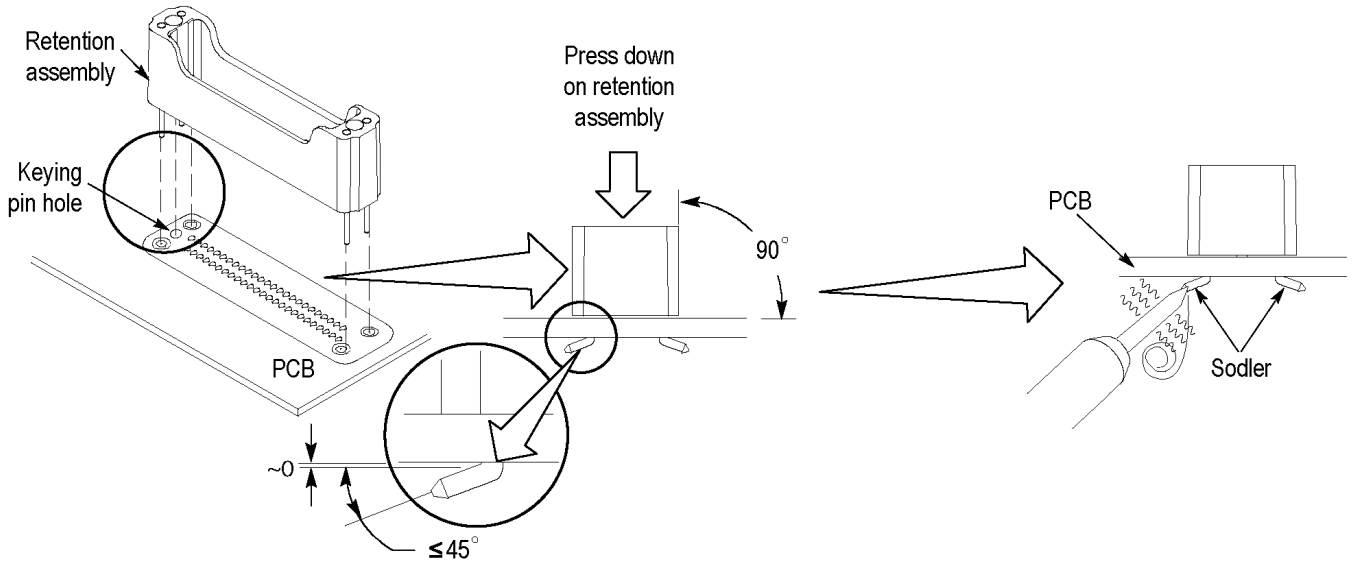
P68xx Standard Accessories

Description	P6810		P6860*5		P6864*5		P6880*5	
	Qty Per Probe	Part Number	Qty Per Probe	Part Number	Qty Per Probe	Part Number	Qty Per Probe	Part Number
Podlet Holders, Bag of 4	1	352-1097-00	–	–	–	–	–	–
1-ch leadset, Single-ended and Differential	2	196-3471-01	–	–	–	–	–	–
8-ch leadset, Single-ended	4	196-3470-01	–	–	–	–	–	–
SMT KlipChip grabber tips, Bag of 20	2	SMG50	–	–	–	–	–	–
Nut bar (used on <0.093 in. thick PCB)	–	–	2	220-0255-00	1	220-0255-00	4	220-0255-00
Elastomer Holder Assembly, Thin (used on <0.093 in. thick PCB), Bag of 2	–	–	1	020-2451-00	1	020-2451-00	2	020-2451-00
Elastomer Holder Assembly, Thick (used on >0.093 in. thick PCB), Bag of 2	–	–	1	020-2452-00	1	020-2452-00	2	020-2452-00
Sheet of Probe Labels	1	335-0345-00	1	335-0346-00	1	335-1017-00	1	335-0697-00

*5 Recommend PEM KFS-256 or equivalent for >0.093 in. thick PCB.

P68xx Optional Accessories

Order Number	Description
TLAHRA	High resistance adapter (18 channels) for P6810
020-2457-00	Mictor-on-PCB to P6860 Probe Adapter
020-2453-00	Nut bar for Thin Elastomer Holder Assembly (Bag of 2)



P69xx Probe Retention Kit

P69xx Standard Accessories

Description	P6960		P6962 / P6964		P6962DBL		P6980		P6982	
	Qty Per Probe	Part Number	Qty Per Probe	Part Number	Qty Per Probe	Part Number	Qty Per Probe	Part Number	Qty Per Probe	Part Number
Sheet of Probe Labels	1	335-1208-00	1	P6962: 335-1772-00 P6964: 335-1315-00	1	335-1956-00	1	335-1209-00	1	335-1313-00
P69xx Probe Retention Kit	1	020-2908-00	1	020-2908-00	1	020-2908-00	2	020-2908-00	1	020-2908-00
Probe Adjustment Tool	1	003-1890-00	1	003-1890-00	1	003-1890-00	1	003-1890-00	1	003-1890-00
Velcro Cable Manager (Bag of 2)	1	346-0300-00	1	346-0300-00	1	346-0300-00	1	346-0300-00	1	346-0300-00

P69xx Optional Accessories

Order Number	Description
020-2539-00	P69xx Probe Mounting Posts

Service Options

The following service options are offered for the TLA logic analyzer products and probes.

Option	TLA7000 Mainframes	TL7ACx Modules	TLA7Bxx Modules	P68xx/P69xx Probes	TLA7Sxx Modules	P67xx Probes
Opt. CA1 provides a single calibration event or coverage for the designated calibration interval, whichever comes first	x	x	x	x	x	x
Opt. C3 Calibration Service, 3 Years	x	x	x	x	x	x
Opt. C5 Calibration Service, 5 Years	x	x	x	x	x	x
Opt. D1 Calibration Data Report	x	x	x			
Opt. D3 Calibration Data Report, 3 Years (with Opt. C3)	x	x	x			
Opt. D5 Calibration Data Report, 5 Years (with Opt. C5)	x	x	x			
Opt. R3 Repair Service, 3 Years	x	x	x	x	x	x
Opt. R5 Repair Service, 5 Years	x	x	x	x	x	x
Opt. S1 On-site service, 1 Year	x					
Opt. S3 On-site service, 3 Years (with R or C options)	x					
Opt. R1PW Repair Service Coverage, 1-year Postwarranty	x	x	x	x (Not P6982)	x	x
Opt. R2PW Repair Service Coverage, 2-years Postwarranty	x	x	x	x (Not P6982)	x	x
Opt. R3DW Repair Service Coverage, 3 Years (includes Product Warranty Period). 3-year period starts at time of instrument purchase	x	x	x	x (Not P6982)	x	x
Opt. R5DW Repair Service Coverage, 5 Years (includes Product Warranty Period). 5-year period starts at time of instrument purchase	x	x	x	x (Not P6982)	x	x

TLA7000 Series Upgrades

You can add new capabilities to your existing TLA mainframe or increase the state speed, memory depth, or add full analog multiplexer capability (TLA7ACx only) to existing TLA modules by ordering the appropriate upgrade kit. Please refer to the TLA Family Upgrade Guide for further details.

CE

ISO 9001

Product(s) are manufactured in ISO registered facilities.

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For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit **www.tektronix.com**

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