1240/*NEW* 1241

GPIB IEEE-488 The 1240/1241 comply with IEEE Standard 488-1978 and with Tektronix Standard Codes and Formats.

Total Design Support: Hardware, Software, and Integration

1241's Color Display Enhances User Interface See page 42B

Up to 72 Acquisition Channels

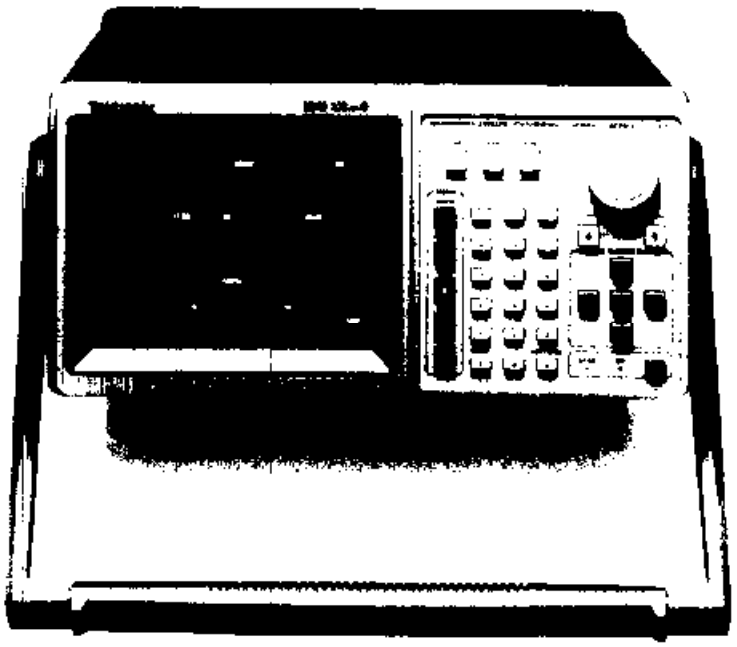
Acquisition Speeds to 100 MHz Async, 50 MHz Sync

14 Levels of Triggering with Conditional Branching

Dual Time Base Triggering, Acquisition and Display

Simple Menu Operation with On-Screen Soft Keys

Transfers Easily into Manufacturing and Service



TOTAL PERFORMANCE

With the 1240/1241 Logic Analyzers, the key phrase is **total performance.** These instruments provide complete support for all aspects of the design task, including hardware analysis, software analysis, and integration.

The *NEW* 1241 color mainframe and 1240 monochrome mainframe provide rapid set-up and operation. Use of either instrument is made simple through a straightforward menu-oriented approach, combined with multi-level operation and touch-screen soft keys. Multi-level operation allows the user to select from one of four levels best matched to the user's skill level and the task at hand. Touch-screen soft keys provide high-level commands at a keystroke, keeping operator selections simple and well labeled.

For hardware analysis, the 1240/1241 offer 100 MHz sampling, glitch triggering and autorun mode. Software analysis is supported by up to 72 channels, sophisticated clocking and 14 level triggering. These capabilities can be tied together through the unique dual time base feature to greatly speed hardware/software integration.

Both the 1241 with its LCCS (Liquid Crystal Color Shutter) display, and the 1240 have configurable architectures each with four card slots which accommodate any combination of 9 channel (1240D1) and 18 channel (1240D2) data acquisition cards, with a maximum of 72 channels. Data analysis and communications capabilities may be added through a series of plug-in ROM and COMM packs.

Hardware Analysis

For hardware analysis, the 1240/1241 offer up to 36 channels of acquisition at sampling rates of 100 MHz asynchronous and 50 MHz synchronous (see acquisition card descriptions). 6 ns glitch detection is also available.

Standard memory depth is 512 bits per channel, and this can be extended to a maximum of 2048 bits per channel by using a special memory chaining feature. This feature allows you to chain one card's memory to another, trading channel width for memory depth.

Superior hardware triggering capabilities include data and glitch triggering for isolating the problem area, clocked and unclocked triggering for capturing events that might not coincide with sample points; and counters, timers, and duration filters for triggering on the characteristics of a signal as well as its occurrence.

Auto-run capability is also provided. This feature allows you to track intermittents through continuous acquisitions. During the acquisitions, you can change parameters on the system under test and dynamically monitor their effects.

Software Analysis

Software analysis is supported by up to 72 data channels at sampling rates of 50 MHz synchronous/asynchronous (see acquisition card descriptions). A flexible clocking scheme includes data demultiplexing without double-probing.

Powerful software triggering capabilities are provided so you can track program flow. Included are 14 trigger levels, conditional branching, counters, timers, and both program flow and data flow qualification. These functions are implemented in two independent event recognizers.

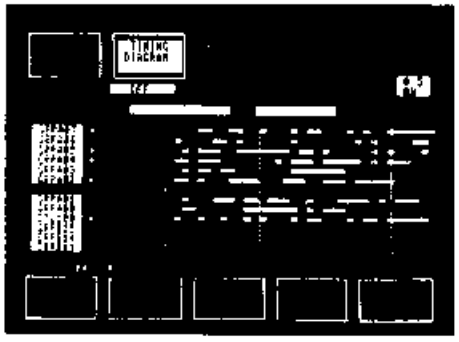


Figure 1. Timing Diagram With Glitches

Figure 2. State Table Display

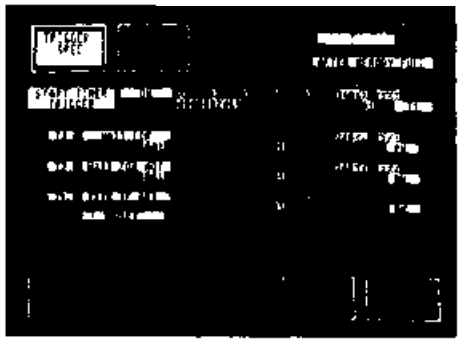


Figure 3. Trigger Specification Menu

Other features that assist in software analysis are flexible channel groupings for display, standard display radices (including ASCII and EBCDIC), and an eight-level pattern search and memory compare with highlighting.

Hardware/Software Integration

For integration, the 1240/1241 offer a dual time-base system that brings together all of the above hardware and software analysis capabilities. This dual time-base system greatly speeds the hardware/software integration process since the acquisition, triggering, and display of two independent time bases are tied together. You can fully monitor the interaction between hardware and software, or monitor the relationship of two interdependent systems. All data displays are time-aligned and completely correlated. The dual time base allows you to integrate functional modules, an increasingly important design task.

FLEXIBILITY NOW AND IN THE FUTURE

The power of the 1240/1241 stem from its configurable mainframe. This mainframe houses a selection of data acquisition cards and plug-in ROM and COMM Packs. You can select features that meet your current application needs, then later upgrade the mainframe to increased performance.

Selectable Acquisition Cards

The 1240/1241 mainframes provide four card slots that accommodate any combination of the following card types: 1240D1 and 1240D2.

The 1240D1 is a 9 channel data acquisition card that can sample at rates up to 100 MHz asynchronous and 50 MHz synchronous. This card also provides glitch capture down to 6 ns, on all channels.

The 1240D2 card is an 18 channel data acquisition card that can sample at rates up to 50 MHz asynchronous/synchronous. Another feature of this card is single-probe demultiplexing.

ROM Packs for Data Processing

A ROM port on the side of the 1240/1241's mainframe supports the addition of special software ROM Packs. With the 1240/1241's acquisition capabilities, you have the capability to capture data which is very specific to your problem at hand. ROM Packs provide a means of helping you analyze that data, by processing it and presenting it to you in the most useful manner. Currently, there are ROM Packs supporting performance analysis, mnemonic disassembly of popular microprocessors, and special communications applications (see pages 116 to 118).

COMM Packs for External Communications

Communication capabilities can be added to the 1240/1241 by inserting COMM Packs into a communications port on the rear of the instrument. These COMM Packs act as adaptors, allowing the 1240/1241 to function in different communication environments including RS-232C and GPIB (see pages 117 and 118).

EASE OF USE

In line with Tek's goal of easy-to-use logic analyzers, the 1240/1241 human interface has been designed to facilitate the user's operation of the instrument.

Menu Operation and Soft Keys

Ease of use starts with the 1240/1241's menu operating system. Straightforward menu displays and on-screen soft keys allow you to make setup choices on the screen where your attention is already directed. You are not distracted by the need to look elsewhere on the instrument.

Multiple Operation Levels

Another major feature of the menu operating system is user-selected operation levels. The 1240/1241 provide four operation levels, ranging from basic operation for simple applications to full operation for complex applications. The sophistication of system features increases with the operation levels.

Configurable from the Front Panel

The 1240/1241 are completely configurable from the front panel, thus eliminating the need to switch boards and reconnect probes when changing from hardware to software applications. Probe connections are on the side of the instrument so they can be easily accessed. The keyboard has a simple layout, with single function keys. Also, a knob is included on the keyboard for data scrolling. This knob, along with the extreme smoothness of the data scrolling, make the 1240/1241 displays easier to read and manipulate.

Figure 4. Scroll Knob.

Automatic Nonvolatile Storage

A battery-backed CMOS memory stores two complete instrument setups, including the last setup used before the 1240 and 1241 are powered down. This facilitates quick instrument start-up when returning to work, and eliminates the problem of losing a setup as a result of power system interruptions.

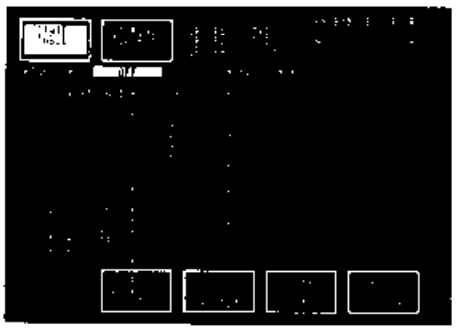


Figure 5. State Table Display with Dual Time-base Acquisition.

Figure 6. Operation Level Menu.

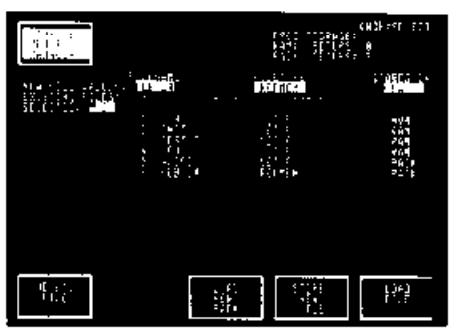


Figure 7. Storage Memory Manager Menu.

IDEALLY SUITED FOR ENGINEERING, MANUFACTURING, AND SERVICE

In addition to its usefulness in the engineering environment, the 1240/1241 is well suited for manufacturing and service tasks. It transfers easily from one environment to another and helps facilitate communications between the different groups through its portability, remote control, mass storage and teleservicing capabilities.

Portability

The 1241 weighs 12.7 kg (28.0 lb) and meets environmental Class 5 specifications. The 1240 weighs 12.0 kg (26.5 lb) and meets environmental Class 3 specifications.

Remote Control

RS-232C and GPIB COMM Packs (see page 117) are ideally suited to automated test environments and remote control.

Mass Storage

Mass storage of setups, acquisition memories, and reference memories is achieved through RAM and EPROM Packs. This type of pack storage allows engineering to easily transfer knowledge to other groups. They can create the setups and memories needed for design test in manufacturing, or they can create servicing procedures at the factory that can be sent out to field service sites.

Two types of pack storage are available. First, there is the 12RS01 8 k RAM Pack and the 12RS02 64 k RAM Pack. Storage and retrieval of information from this RAM Pack is accomplished via menu soft keys (see Figure 7). The 12RS11 32 k EPROM Pack (no EPROMs included) and the 12RS12 32 k EPROM Pack (EPROMs included) provide a permanent storage medium for setups and memories. To store files on these EPROM Packs, the setups and memories are uploaded from the 1240/1241 to a host computer via GPIB or RS-232C and then burned into EPROMs.

Teleservicing

Master-Slave capability allows one 1240/1241 to remotely control another over a telephone line (see page 119). This greatly eases the higher levels of service troubleshooting, as service specialists can get to the problem via the telephone rather than having to physically travel to the problem site.

12RMXX

Series Microprocessor Support

Twenty-one Processors Supported

Single-Plug Connection for Ease of Use and Reliability

State Table Display in Four Formats: State, Absolute, Hardware and Software

Cursor Readout in Timing Diagram Displayed in Disassembly Format

The 1240/1241 provide microprocessor support for major 8-bit, 16-bit and 32-bit processors. This support includes a single plug interface, data acquisition capability and mnemonic disassembly.

For simple 8 bit and 16-bit processors, the 1240/1241 use general purpose clocking and demultiplexing capabilities to acquire the data for disassembly by the 12RMXX. Two 1240D2 cards using standard data acquisition probes (P6460 or P6462) are attached to the processor via a probe interface. See page 121 for information on the Configured Probe Interface. Three 1240D2 cards are required for the simple 16-bit processors.

For more complex 8 bit, 16-bit and 32-bit processors, the 1240/1241 use the PM200 Series of personality modules to interface to the processor and acquire the data for disassembly by the 12RMXX. These modules provide the special purpose hardware needed to properly acquire the instruction flow from a prefetch processor architecture and its associated internal queue. These modules plug directly into the 1240D2 cards, replacing the data acquisition probes and providing the interface to the processor. Three 1240D2 cards are required for these more complex processors. See page 121 for information on the PM 200 Series.

The microprocessor disassembly support for the 1240/1241 are in the form of Mnemonics ROM Packs (12RMXXs), with one ROM Pack for each microprocessor.

Four disassembly formats are available for viewing the data after disassembly: State, Absolute, Hardware, Software (only two display formats are available for the 68020: State and Absolute).

State format is exactly the same as standard State Table format.

Absolute format augments the State format with cycle operation labels (FETCH, WRITE, etc.).

Hardware format provides disassembly information for all cycles occurring on the bus (instructions or cycle labels on all acquired cycles.)

Software format displays the executed instructions. It is similar to Hardware disassembly format with the display of instruction read cycles which are not opcode fetches suppressed. DMA's and flushed instructions are also suppressed.

The processors that are currently supported by the 1240/1241 are:

6800	8080	6502/65C02
6802	8085	NSC 800
6808	8086	Z80
6809	8088	Z8001
68000	80186	Z8002
68008	80188	F9450
68010	80286	
68020		

For ordering information, please refer to the Microprocessor Support section on page 121.

12R01 Performance Analysis

Two Types of Analysis: State Overview and Event Measurements

Monitor Memory Use, Execution Cycles, Subroutine Calls

Measure Time or Occurrences

Compare Statistics on Four Events, Analyze Distribution of Single Event

Measure Events Using Two Independent Time Bases

Performance analysis is a tool that assists engineers in the development of microprocessor based products. It can be used throughout the life cycle of a product to help the designer characterize, test, debug, and optimize software and system activity.

The real benefit of performance analysis over other types of development tools is that it provides nonintrusive overview measurements of system performance. In other words, it can be used to improve efficiency by providing measurements that characterize system performance without altering the performance.

The 12R01 Performance Analysis ROM Pack provides two types of performance analysis, State Overview and Event Measurement, for the 1240/1241. These two types of analysis provide overviews of the activity of the system under test, graphically displaying this activity in the form of histograms.

State Overview

With State Overview, the user can acquire data on a set of defined ranges. Each range has a lower-bound value and an upper-bound value and is defined for a specific group from the Channel Grouping menu. After a data acquisition is made (using the standard 1240/1241 triggering) each cycle of the acquired data is searched to find any matches between the channel groups and the ranges defined for them. A match occurs any time the value of a group at a given cycle is greater than or equal to the lower-bound value and less than or equal to the upper-bound value of a range associated with that group.

Figure 8. 80186 Software Format.

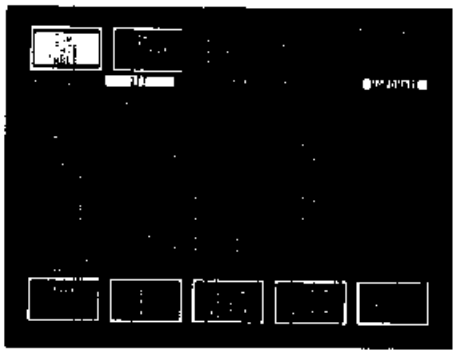


Figure 9. Z80 Hardware Format with dual timebase acquisition.

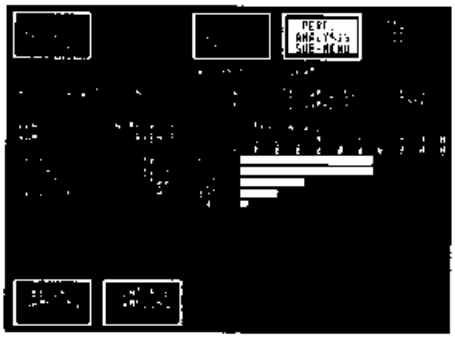


Figure 10. View range histograms menu.

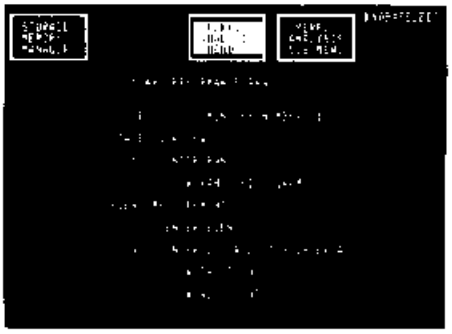


Figure 11 Performance Analysis Menu

A cumulative count of the matches is kept for each range, and that count is displayed as a total count, a percentage of the total number of acquisition cycles on the associated channel group's given time base, and as a bar graph (histogram) proportional in length to that percentage. Up to eleven ranges can be defined.

Event Measurement

With Event Measurement, the user is able to delimit the events that are to be analyzed. A measurement in this type of analysis consists of a start measurement event, an optional target event and a stop measurement event. The data acquired in a single occurrence of the start measurement/stop measurement cycle is defined as a "sample". When sampling begins, the 1240/1241 repeatedly takes the same kind of measurement sample until the user stops the instrument. Within each sample, some type of measurement takes place, and this information is then processed for display.

The target event may be a single event that the user wishes to count occurrences of or time. It can also be two events, in which case the 1240/1241 will measure the time between them. If no target event is chosen, the duration of each sample can be timed, or the number of clock cycles that occur on a given time base during each sample can be counted. Up to four events can be defined.

1200CXX, 12RCXX

Communications Support

Line Printer Support for Most Printers

Master/Slave Support

Three Communication Interfaces

External communication capability is supported in the 1240/1241 by means of modular COMM Packs. These COMM Packs, which plug into a COMM port on the back provide flexibility in interfacing other equipment.

REMOTE CONTROL

Two COMM Packs are provided to interface the 1240/1241 to controllers, the 1200C01 RS-232C COMM Pack and the 1200C02 GPIB COMM Pack. You can remotely control all of the capabilities of the 1240/1241 using these COMM Packs.

The controller can start and stop data acquisitions and the auto run function, write to the display, define custom soft keys, request 1240/1241 keystrokes, and initiate and request diagnostic results. Instrument setups, acquisition memories, reference memories and RAM Pack contents can be sent and received from the 1240/1241, also.

Requests from the 1240/1241 to upload and download setups and memories are initiated via soft keys (see figure 14).

The 1200C02 GPIB COMM Pack interface conforms to IEEE specification 488-1978, Standard Digital Interface for Programmable Instrumentation. The 1240/1241 operates via the GPIB COMM Pack with the Tek 4041 controller.

PRINTER SUPPORT

Through the use of a ROM Pack and COMM Pack combination the 1240/1241 are able to print hard copies of setup menus and data acquisition memories. Support will be provided for almost all commercially available low-cost printers (see figure 15).

The printer interface consists of the combination of a ROM Pack and a COMM Pack. The 12RC01 Printer Support ROM Pack is used in combination with either the 1200C01 RS-232C COMM Pack (for printers with a serial interface) or the 1200C11 Parallel Printer COMM Pack (for printers with a parallel interface).

Nearly all screen displays can be printed including Operation Level, Time Base, Memory Configuration, Channel Grouping, Trigger Spec, Auto-Run Spec, State Table, and Timing Diagram. In addition, a special combined state and timing format is available.

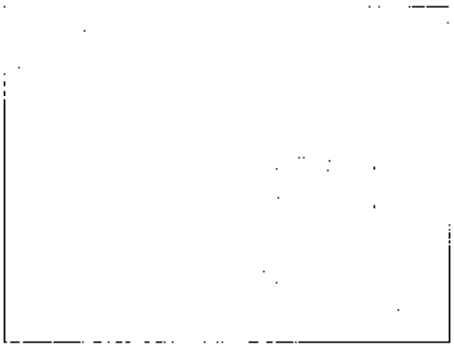


Figure 12 Combined Format Print-out

The Printer ROM Pack also has the ability to print a single display as it appears on the screen. Other functions available are the search pattern, user defined timing trace labels up to 45 characters long for timing diagram printouts, and a printer test to check connections and printer operation.

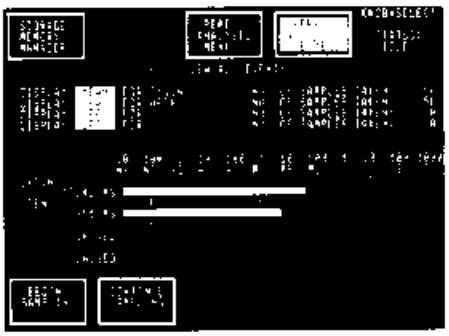


Figure 13 View all events menu.

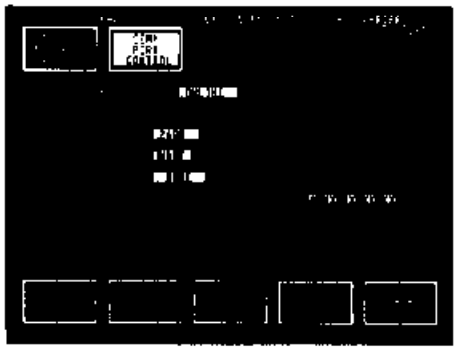


Figure 14. COMM Port Control menu with a 1200C01 RS-232C COMM Pack installed.

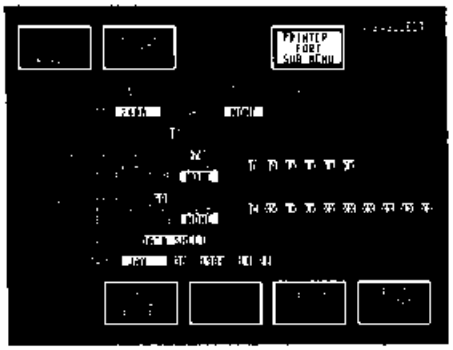


Figure 15 Printer Port sub-menu for setting up printer interface parameters.

TELESERVICING

Master-Slave capability allows one 1240/1241 to remotely control another over a telephone line. This greatly eases the higher levels of service troubleshooting, as service engineers can get to the problem via the telephone rather than having to physically travel to the problem site.

A phone link between the master 1240/1241 and the slave 1240/1241 can be used for sending both data and voice information. When in data mode, the master 1240/1241 has complete control over the slave, with the ability to: send and receive set-ups, acquisition memories and reference memories, start and stop acquisitions, start and stop auto-acquisition, receive information on whether the memories were equal or not equal after auto-acquiring; initialize the slave; get the slave's status; and have the slave call the master when an acquisition or auto-acquisition is over.

In voice mode, the service engineer at the master 1240/1241 can speak directly with the technician at the slave end and direct him to move probes or to swap boards. Switching between voice and data mode is accomplished through the master/slave menu when the Option 01 modem is used.

Also available with the Option 01 modem are auto-answer and auto-dial. With auto-answer, an unattended 1240/1241 will respond to a call from another 1240/1241. A master/slave connection can thus be set up without a service technician present at the slave end.

With auto-dial, a slave 1240/1241 can be set up to automatically call the master upon triggering. If troubleshooting an intermittent problem, the slave can be set to trigger on the problem, the service technician can leave the slave site, the line can be disconnected, and when the intermittent occurs, the slave will call the master, and the service engineer can analyze the data.

The 1240/1241 supports master/slave operation with the following configuration: A 12RC02 Master/Slave ROM Pack, a 1200C01 RS-232C COMM Pack and a modem.

Each 1240/1241 must have at least one acquisition card (1240D1 or 1240D2) installed. Once the connection between the master and a slave is established, the master will assume the card configuration of the slave until it's power is turned off or until a connection is established with another slave.

The Option 01 Hayes Smartmodem 1200 is recommended for use with master/slave support in the United States and other countries where it is licensed. With this modem, the user has access to the following features through the front panel: auto-dial of up to four phone numbers, auto-answer, and soft key switching between voice and data communication modes. This modem is not licensed in all countries, however in these countries the 12RC02 and 1200C01 can be used with many full-duplex modems. With modems other than the Hayes Smartmodem 1200, the telephone connection must be made by hand, and auto-dial, auto-answer, and soft key switching between voice and data modes do not function.

EXTERNAL COMMUNICATION SUPPORT

To equip the 1240/1241 for one of the three types of communications support shown across the top of this table, choose one of the combinations of ROM Pack and COMM Pack whose intersection is indicated by XXXX's. Performance varies depending on the combination of packs that you select for a particular kind of support.

	Remote Control	Printer Support	Master/ Slave Support
ROM Packs	None Required	12RC01 Printer Support	12RC02 Master/ Slave
COMM Packs			
1200C01 RS-232C	XXXX	XXXX	XXXX
1200C02 GPIB	XXXX		
1200C11 Parallel Printer		XXXX	

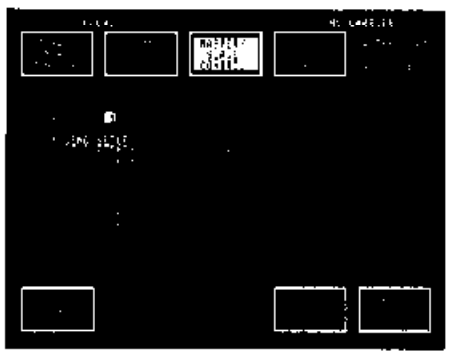


Figure 16. Master/Slave Control Menu.

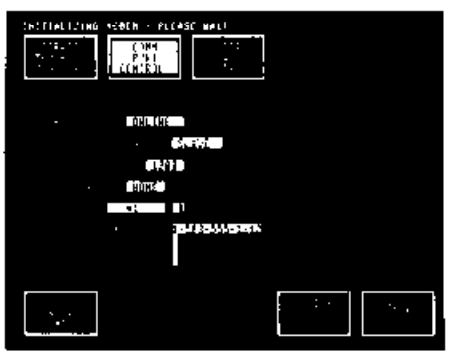


Figure 17. Comm Port Control Menu.

TEK LOGIC ANALYZERS

CHARACTERISTICS

Characteristics are common to the 1240/1241 unless otherwise indicated

OPERATING LEVELS

Level 0 — Basic Operation.
Level 1 — Advanced timing analysis (includes basic state analysis).
Level 2 — Advanced state analysis (includes basic timing analysis)
Level 3 — Full operation.

TIME BASES

Two Per Instrument — Assignable by probe
Time Base 1: Asynchronous or Synchronous
Time Base 2: Synchronous or Demultiplex

INPUTS

Clocks — C1, C2, . . . Cn Where n = number of probes = number of channels/9. Minimum Pulse Width: 8 ns. Specifiable as rising, falling, or either edge.

Qualifiers — Q1, Q2, . . . Qn Where n = number of probes = number of channels/9. Setup Time, Hold Time: = (P6460) 11 ns, 0 ns, (P6462) 17 ns, 6 ns. Specifiable as high or low level

Asynchronous — Rate: 1240D1: 10 ns to 1 s, (1240D2: 20 ns to 1 s). Specification: (1-2-5 sequence) • (Q1 • Q2 • . . . • Qn). Accuracy: 0.01% Channel-to-Channel Skew: ± 3 ns. Glitch Detection: (1240D1 only) 6 ns

Synchronous — Rate: Dc to 50 MHz. Setup Time, Hold Time: On 1240D1 is (P6460) 7 ns, 2 ns; (P6462) 12 ns, 7 ns. On 1240D2 is (P6460) 12 ns, 0 ns; (P6462) 17 ns, 5 ns. Specification: (C1 − C2 − . . . − Cn) • (Q1 • Q2 • . . . • Qn). Minimum Delay After Previous Clock: 20 ns

Demultiplex — Rate: Dc to 50 MHz. Setup Time, Hold Time: On 1240D1 is (P6460) 7 ns, 2 ns, (P6462) 12 ns, 7 ns. On 1240D2 is (P6460) 12 ns, 0 ns, (P6462) 17 ns, 5 ns. Specification: First Phase Clock (Latch Data): (C1 + C2 + . . . + Cn) • (Q1 • Q2 • . . . • Qn). Minimum Delay After Last Phase Clock: 20 ns. Last Phase Clock (Store Data): (C1 + C2 + . . . + Cn) • (Q1 • Q2 • . . . • Qn). Minimum Delay After First Phase Clock: 10 ns

CONFIGURABILITY

Two types of acquisition cards: 1240D1, 1240D2. Maximum of four cards per 1240/1241, in any combination.

	1240D1	1240D2
Number of Channels	9	18
Asynchronous Rate	100 MHz	50 MHz
with glitches	50 MHz	N/A
Synchronous Rate	50 MHz	50 MHz
Memory Depth (Bits/Char Channel	512	512
with Glitches	256	N/A
Max Via Chaining	2048	2048

Depth vs Channels — Tradeoffs possible between data acquisition cards of same type. Maximum depth is 2048 (with four 1240D1 or four 1240D2)

DATA ACQUISITION

Two Types of Acquisition Probes: P6460, P6462
One probe required per 1240D1, two per 1240D2.

	P6460	P6462
Signal Input		
Data Channels	9	9
Clock/		
Clock Qualifier Lines	1	1
Impedence		
Nominal	1 MΩ, 5 pF	TTL/CTTL
Threshold Range	+6.35 V to +6.35 V	+1.4 V
Increments	0.05 V	—
Accuracy	± 0.5% ± 0.065 V	± .25 V ± .055 V; 10°C – 25°C
Threshold Assignment	By acquisition card	N/A
Polarity Assignment	By channel	By channel
Maximum Input Voltage		
Peak	± 40 V	2 to −7 V
Channel to Channel	± 80 V	No restriction

NOTE: All system specifications are based upon P6460 probes; for specifications based upon P6462 probes, please refer to the 1240/1241 Data Sheet

TRIGGER DEFINITION (TWO EVENT RECOGNIZERS)

Global Event Recognizer (Event Recognizer #1) — One level. Event Recognition specified by: Word recognizer—data (data or glitch on 1240D1). Duration filter—1 to 16 consecutive samples or 10 ns to 160 ns. Commands: Store On (Not), Trigger On (Not), Reset On (Not), Start Timer On (Not), Time While On (Not), Increment Counter On (Not), or Off. Counter-timer: Clock interval is 10 ns. Range is 0 to 99,999,999,999 (either counts or 10 ns increments). Counter-timer value may be used to cause trigger or reset.

Sequential Event Recognizer (Event Recognizer #2) — 14 levels. Event Recognition on Each Level Specified By: Time Base: Which time base to monitor for event. Word Recognizer: Data (data or glitch on 1240D1). Iteration Counter: 1 to 9999 occurrences. Duration Filter: 1 to 16 consecutive samples. Selective Storage on Each Level Specifiable: With Storage On or with Storage Off. Commands on Each Level: Wait For (Not), Trigger If (Not), Reset If (Not), Jump If (Not) or Delay (up to 9999). Commands at End of Sequence: Trigger, Reset or Do Nothing.

External Trigger Out — TTL level output whenever trigger attempted

External Trigger In — TTL level input can be required for enabling trigger

AUTORUN

Modes of Operation — Compare Acquisition Memory to Reference Memory. Specifiable which channels to compare, specifiable starting and ending memory locations of comparison. Result of Comparison Outcome: Specifiable display and reacquire, discard and reacquire or display and stop. Specifiable Minimum Display Time: 0 s to 99 s

Continuous Trigger Out — Data is not stored. 1240/1241 acts as trigger source

Trigger In — Requires trigger in signal to enable trigger. Enables two 1240/1241s to work in parallel.

Store After Trigger — Data at last trigger is available after stopping 1240/1241. Time between storages is minimum.

DISPLAY FORMATS

State Table — Acquisition or reference memory. Data displayed in binary, octal, hex, ASCII, EBCDIC. Glitch display can be turned on or off

Timing Diagram — Acquisition or Reference Memory. Horizontal Expansion: *1, *2, *5, *10, *20. Vertical Expansion (1241 only): *1, *2.

Distance Between Cursors — Value displayed as absolute time for unqualified asynchronous measurement, as number of memory locations for qualified or synchronous measurement

Highlighting Modes — Memory comparison differences, glitches, search pattern occurrences, time base #1 occurrences, time base #2 occurrences.

Search Pattern — Length: 1 to 8 contiguous locations. Time Bases: Can restrict each location to occur only on T1, T2 or T1 and T2.

STORAGE

Internal (Standard)

Nonvolatile Memory (NVM) — Size: Contains two set-ups, including status at power down. Lithium iodide battery

Volatile Memory (RAM) — Size: Contains two set-ups

Memory Types

Set-Up — Stored in NVM, RAM, or Pack, contains all data pertinent to making an acquisition

Reference Memory — Stored in Pack, reference memory is editable in Edit Reference Memory menu.

ENVIRONMENTAL CHARACTERISTICS

Temperature — Operating: (1240 only) −10°C to +55°C, (1241 only) 0°C to 50°C. Nonoperating: −62°C to +85°C

Altitude — Operating: To 4600 m (15,000 ft). Nonoperating: To 15,000 m (50,000 ft)

Vibration — 0.025 inch displacement, 10 Hz to 55 Hz frequency range

Shock — 30 g

OTHER CHARACTERISTICS

Diagnostics — At power-up, the 1240/1241 performs processor, ROM, RAM and board checks. A test pattern generator located on the side provides stimulus for verifying probes and acquisition system operation. Complete system verification and extended diagnostics are available with an optional ROM Pack

Rear Panel Connections — Trigger In: TTL compatible. Trigger Out: TTL compatible. Video Out: (1240 only) Conforms with RS-170 (composite video)

Power — 90 V to 132 V or 180 V to 250 V, 48 Hz to 63 Hz
NOTE: 48 Hz to 440 Hz operation with addition of safety ground strap

PHYSICAL CHARACTERISTICS

Dimensions	mm	in
Width	368	14.5
Height	197	7.8
Depth	498	19.6
Weight	**kg**	**lb**
Without Accessories	12.0	26.5

COMM Packs

1200C01 (RS-232C) — Baud Rate: 110 to 9600 Bits/Character: Eight, including parity bit. Protocol: Asynchronous full duplex. Compatability: Stand-alone with host for remote control with 12RC01 for printers with serial interface, with 12RC02 and 12RC02 Option 01 for master/slave, with 12RMXX for printers with serial interface.

1200C02 (GPIB) — Full listener/talker capabilities. Meets IEEE Standard 488-1978. Compatability: Stand-alone with host for remote control

1200C11 (Parallel Printer) — Compatability With 12RC01 for printers with parallel interface with 12RMXX for printers with parallel interface

ROM Packs

Analysis

12R01 (Performance Analysis) — State Overview: 1 to 11 ranges. Ranges can be different groups and different timebases. Ability to halt and resume measurement. Display in count, percentage, and histogram. Event Measurement: 1 to 11 distribution intervals; 1 to 4 events; 10 ns resolution. Five measurement types (measure total time, count cycles, count occurrences, time occurrence, accumulate time). Display in distribution, min, mean, max, and histogram.

Communication Support

12RC01 (Printer Support) — Requires 1200C01 for serial interface or 1200C11 for parallel interface. Output Menus, search pattern, acquisition and reference memory. Memory Format: State table, timing diagram, and combined.

12RC02 (Master/Slave) — Requires: 1200C01 and modem. With Option 01: Auto-answer, auto-dial, voice-data switching, non-volatile storage of four phone numbers, 300 baud and 1200 baud. Diagnostics: Local 1240/1241 with COMM Pack and RS-232 cable, modem, and link between local and remote 1240/1241.

External Storage (Optional)

12RS01 (8 k RAM Pack) — Size: Contains 8 kbytes with Lithium battery.

12RS02 (64 k RAM Pack) — Size: Contains 64 kbytes with Lithium battery.

12RS11 (32 k EPROM Pack) — Size: Contains 32 kbytes (no EPROMs included). Requires four 68764s or 68766s.

12RS12 (32 k EPROM Pack) — Size: Contains 32 kbytes. Comes with four 68764s or 68766s.

Microprocessor Support

12RMXX (Mnemonic Disassembly) — Formats: State: Absolute, Hardware, Software.

ORDERING INFORMATION

1240 Logic Analyzer Mainframe **$4,500**

Includes: Accessory pouch (016-0707-00), front panel cover (200-2780-00), operator manual (070-4340-01), reference guides (070-4641-01).

1241 Color Logic Analyzer Mainframe **$6,000**

Includes: Same as above

Option 05 — Rackmount Adaptor **+$400**

INTERNATIONAL POWER PLUG OPTIONS

Option A1 — Universal Euro 220 V/16 A, 50 Hz

Option A2 — UK 240 V/13 A, 50 Hz

Option A3 — Australian 240 V/10 A, 50 Hz

Option A4 — North American 240 V/15 A, 60 Hz

Option A5 — Switzerland 220 V/10 A, 50 Hz

STANDARD SYSTEM CONFIGURATIONS

8-BIT

1240N08 — 8-Bit Microprocessor Analysis System **$12,400**

Includes: 1240 Logic Analyzer with two 1240D2 modules with four P6460 probes, 12RS02 RAM Pack.

1241N08 — 8-Bit Microprocessor Analysis System **$13,900**

Includes: Same as above except the 1241 Logic Analyzer

OPTIONS

Options 01 thru 09 — Microprocessor Specific Support (includes 12RMXX Microprocessor Disassembly ROM Pack, 12RMXX Option 01 Configured Probe Interface)

Option 01 — Specific Support for 8080 **+$600**

Option 02 — Specific Support for 8085 **+$600**

Option 03 — Specific Support for 6800 **+$600**

Option 04 — Specific Support for 6802 **+$600**

Option 05 — Specific Support for 6808 **+$600**

Option 06 — Specific Support for 6809 **+$600**

Option 07 — Specific Support for Z80 **+$600**

Option 08 — Specific Support for 6502 **+$600**

Option 09 — Specific Support for NSC800 **+$600**

16-BIT

1240N16 — 16-Bit Microprocessor Analysis System **$12,600**

Includes: 1240 Logic Analyzer with three 1240D2 Option 1D Modules without probes. P6460 Probe, 12RS02 RAM Pack.

1241N16 — 16-Bit Microprocessor Analysis System **$14,100**

Includes: Same as above except the 1241 Logic Analyzer

OPTIONS

Options 01 thru 09 — Microprocessor Specific Support (includes 12RMXX Microprocessor Disassembly ROM Pack, 12RMXX Option 02 or Option 04 Personality Module)

Option 01 — Specific Support for 8086 **+$2,500**

Option 02 — Specific Support for 8088 **+$2,500**

Option 03 — Specific Support for 80186 **+$2,500**

Option 04 — Specific Support for 80188 **+$2,500**

Option 05 — Specific Support for 68000 (DIP) **+$2,500**

Option 06 — Specific Support for 68000 (PGA) **+$2,500**

Option 07 — Specific Support for 68008 **+$2,500**

Option 08 — Specific Support for 68010 (DIP) **+$2,500**

Option 09 — Specific Support for 68010 (PGA) **+$2,500**

GENERAL PURPOSE

1240NGP — General Purpose Analysis System **$15,350**

Includes: 1240 Logic Analyzer with 1240D1 module with P6460 probe, two 1240D2 modules with four P6460 probes, 12PS02 RAM Pack.

1241NGP — General Purpose Analysis System **$16,850**

Includes: Same as above except the 1241 Logic Analyzer

BUS ANALYSIS

1240NBA — Bus Analysis System **$19,800**

Includes: 1240 Logic Analyzer with four 1240D2 modules with eight P6460 probes, 12RS02 RAM Pack.

1241NBA — Bus Analysis System **$21,300**

Includes: Same as above except the 1241 Logic Analyzer.

HIGH SPEED ANALYSIS

1240NHS — High Speed Analysis System **$16,800**

Includes: 1240 Logic Analyzer with four 1240D1 Modules with four P6460 probes, 12RS02 RAM Pack.

1241NHS — High Speed Analysis System **$18,300**

Includes: Same as above except the 1241 Logic Analyzer

OPTIONAL ACCESSORIES

ACQUISITION CARDS

1240D1 — 9-Channel Data Acquisition Card, 100 MHz, includes one P6460 data acquisition probe. **$2,950**

Option 1D — Deletes one P6460 Data Acquisition Probe **−$700**

1240D2 — 18-Channel Data Acquisition Card, 50 MHz, includes two P6460 data acquisition probes **$3,700**

Option 1D — Deletes two P6460 Data Acquisition Probes. **−$1,400**

Option 2S — Substitutes two P6462 Data Acquisition for two P6460 Data Acquisition Probes **−$720**

DATA ACQUISITION PROBES

P6460 — 9 Channel Data Acquisiton Probe **$700**

P6462 — 9-Channel Data Acquisiton Probe, fixed threshold TTL **$340**

COMMUNICATION INTERFACES

COMM PACKS

1200C01 — RS-232C COMM Pack **$750**

1200C02 — GPIB COMM Pack **$850**

1200C11 — Parallel Printer COMM Pack **$500**

Note: To order cables for these COMM Packs, see the Logic Analyzer Accessories Section.

ROM PACKS

Analysis

12R01 — Performance Analysis ROM Pack **$800**

Communication Functions

12RC01 — Printer Support ROM Pack **$300**

12RC02 — Master/Slave ROM Pack **$500**

Option 01 — Modem. **+$600**

Storage

12RS01 — 8 k RAM Pack **$300**

12RS02 — 64 k RAM Pack **$500**

12RS11 — 32K EPROM PACK (Empty) **$85**

12RS12 — 32K EPROM PACK **$300**

SERVICE ACCESSORIES

12RD01 — Diagnostic ROM Pack **$1,500**

Diagnostic Lead Set — Order 012-0556-00 **$50**

Extender Card — Order 670-7539-02 **$400**

Service Manual — Order 062-7124-02 **$150**

Service Maintenance Kit — Includes the above service accessories. Order 067-1103-02 **$2,000**

CARTS

Portable Instrument Cart — For on site portability. Order K212. See page 423 for complete description. **$330**

Instrument Shuttle — For site-to-site portability. Order K117. See page 423 for complete description **$265**